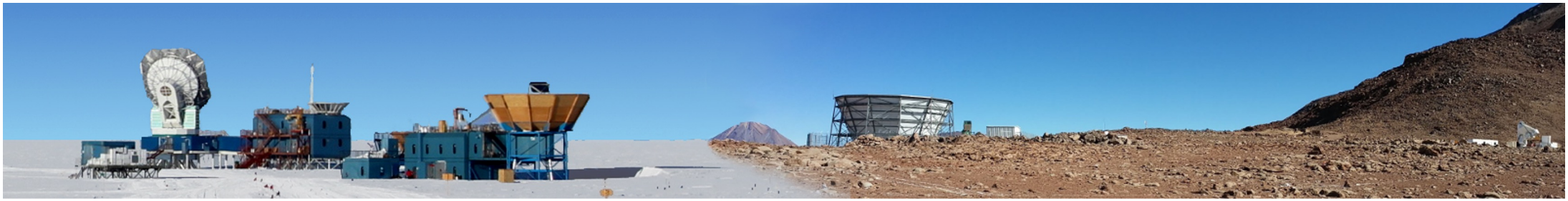


CMB-S4

contribution to the front-end readout chain

Damien PRÊLE

on behalf of the CMB-S4@IN2P3 : **Horacio Arnaldi**(1), James Bartlett (1), Olivier Bourrion(4), Andrea Catalano(4), **Si Chen** (1), Céline Combet(4), Jacques Delabrouille(2), Elena de laHoz(2), Cyrille Doux(4), Josquin Errard(1), Ken Ganga(1), Xavier Garrido(3), **Manuel Gonzalez**(1), Jean-Christophe Hamilton(1), Sophie Henrot-Versillé(3), Julius Hrivnac(3), Marine Kuna(4), Fabian Lambert(4), Sotiris Loucatos(1), Thibaut Louis(3), Juan Macías Pérez(4), Frédéric Mayet(4), Jerôme Odier(4), Julien Peloton(4), Laurence Perotto(4), **Michel Piat**(1), **Damien Prêle**(1), **Fatah Rarbi**(4), Radek Stompor(2), Jean-Pierre Thermeau(1), Steve Torchinsky(1), Matthieu Tristram(3), Christophe Vescovi(4)

(1) AstroParticule et Cosmologie (APC)

(2) Centre Pierre Binétruy (CPB)

(3) Laboratoire de Physique de 2 infinis, Iréne Joliot-Curie, (IJCLab)

(4) Laboratoire de Physique Subatomique et Cosmologie, (LPSC)

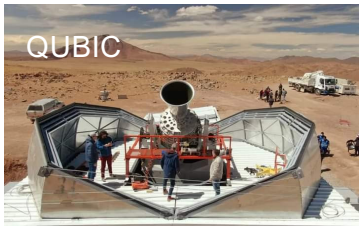
Who Am I

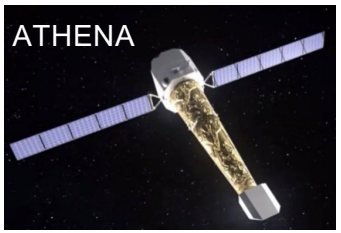
Damien PRÊLE – APC / Univ. Paris Cité

Instrumentalist, VLSI Research Engineer, Project Manager

CMB-S4 project and collaboration member

- **TES/SQUID detection chain projects**
  - Instrumentalist for the **QUBIC** ground based telescope for CMB
  - Project manager Warm Front End Electronic - WFEE - for X-IFU **ATHENA**
    - Co-Investigator member of the X-IFU instrument
    - ATHENA X-IFU detection chain WG
  - IN2P3 instrument leader - **CMB S4** warm analog front-end readout
    - CMB-S4 readout chain WG



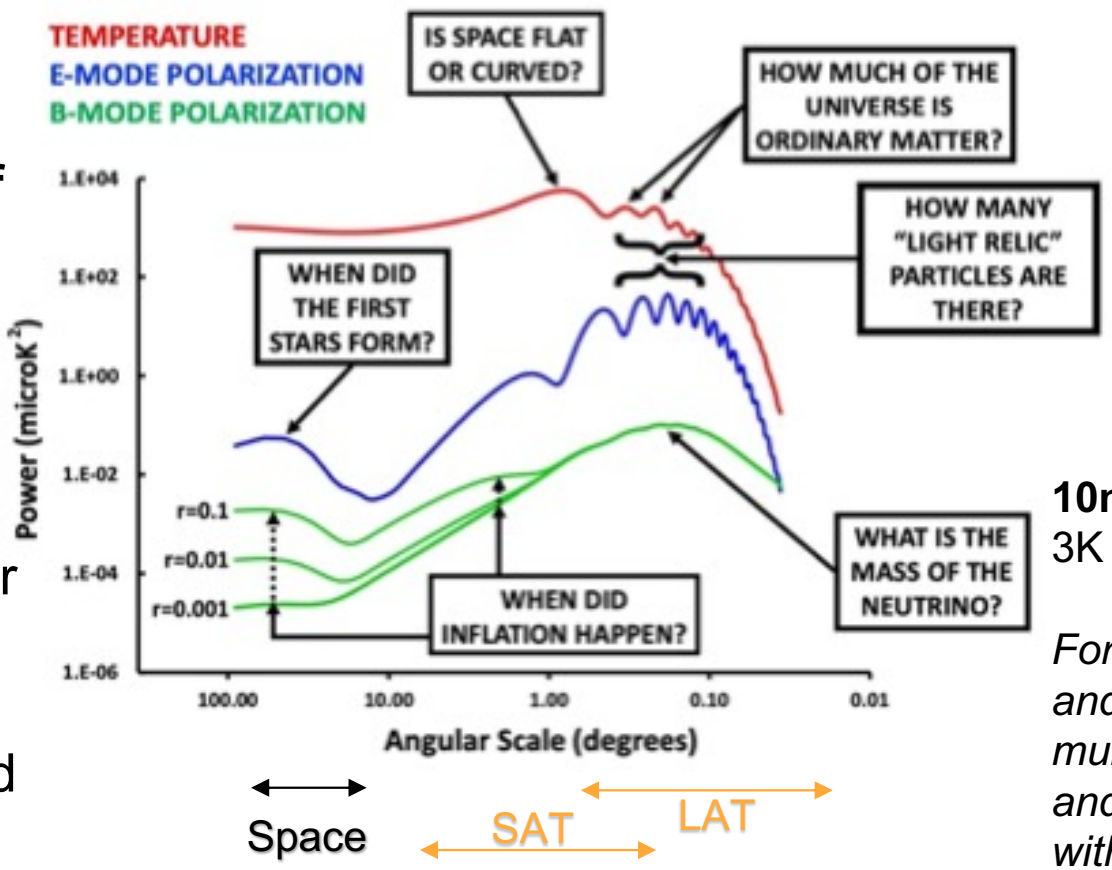


Micro-electronic and BiCMOS SiGe **integrated circuits – ASIC**, Cryo. Semiconductors, Superconductor devices (**SQUID, TES**), Electronic **Noise mitigations and EMI/EMC**, Multiplexing, **Low noise amplifier – LNA**, **Low noise DACs**, Space technology

CMB Angular Power Spectra Guide

Weak anisotropy Encoded in CMB intensity and polarization -> **story of the origin, evolution, and make up of the Universe**.

Need to measure the anisotropy from angular scales of **degrees to arcminutes** with exquisite sensitivity and fidelity.



10nK fluctuations on a 3K in a 300K environment

Foregrounds mitigation and de-lensing requires multiple frequency bands and broad angular range with exceptional sensitivity and control of systematics

CMB-S4 Instrument Description after AoA

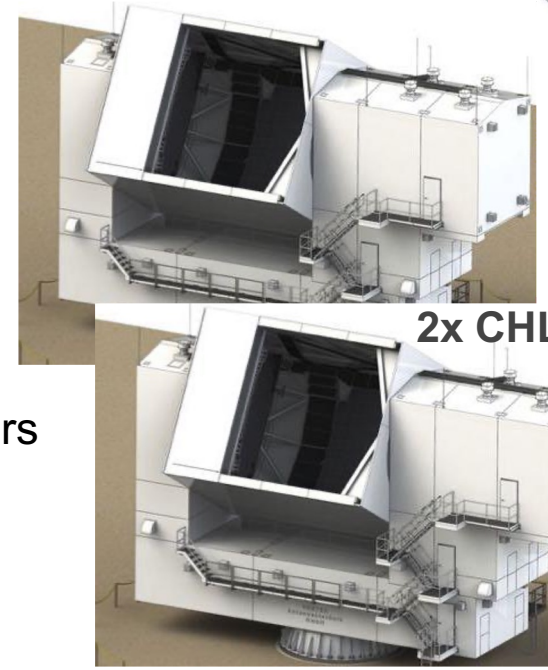
- **500 k deployed detectors** (483344)
- 363 wafers (All wafers are dichroic except the ULF wafer)
- **3 LATs**
  - 2 x 6 m CD* Chile > 50% sky
  - 1 x 5 m TMA** Pole ~3% sky)

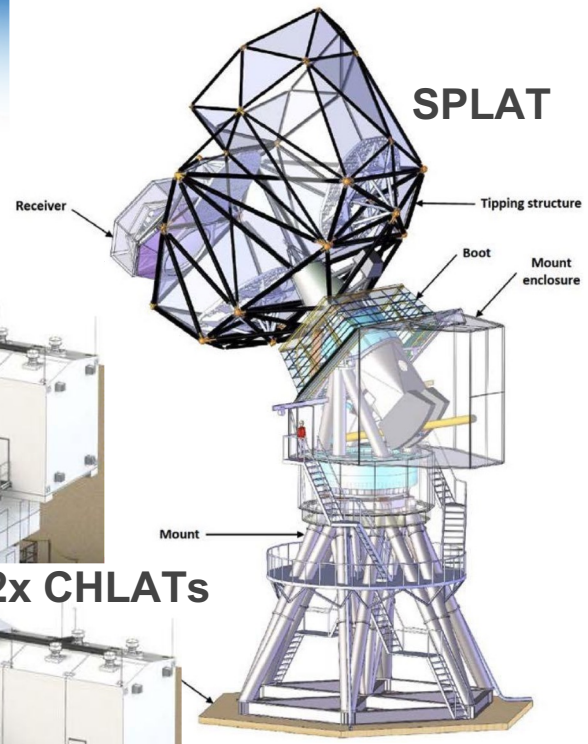
  -> 3x85 tubes$_{20cm}$; 255 wafers ; 400 k detectors

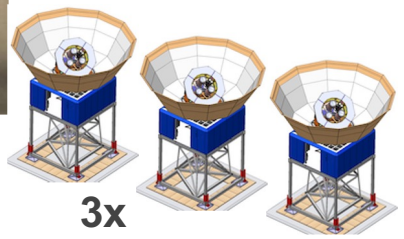
  - 200 TES ULF; 5k LF; **280k MF**; 120k HF
- **3 SATs**

  -> 3x3 tubes$_{50cm}$; 108 wafers ; 80 k detectors

  - 500 TES LF; 40k MF; 40k HF





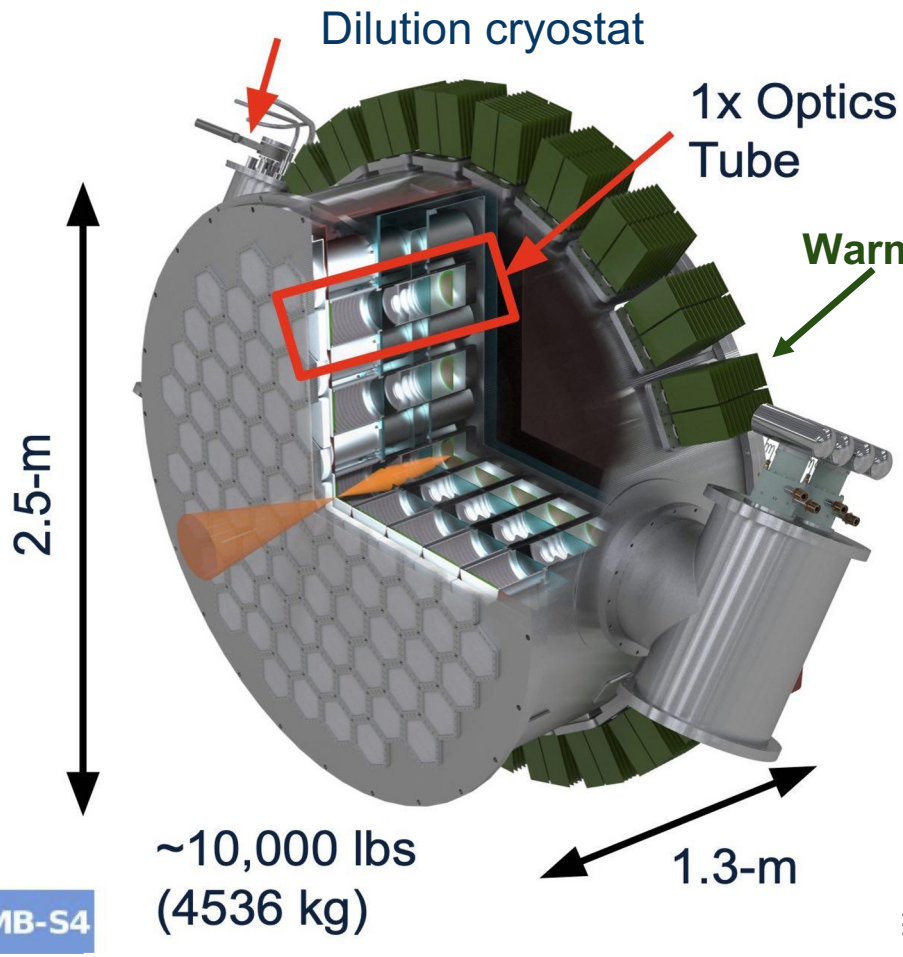


*CD - high-throughput off-axis crossed-Dragone
**TMA - five-meter diameter three-mirror anastimatic telescope

[1] Large Aperture Telescopes Update - M. Niemack
[2] https://cmb-s4.org/experiment/

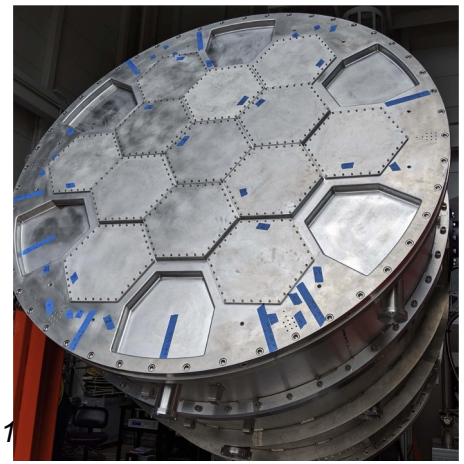
CMB-S4 LAT and SAT receiver cryostat design

LAT - Large Aperture Telescope

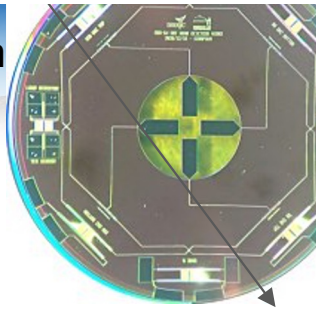


SAT - Small Aperture Telescope

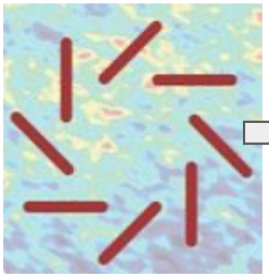
CMB-S4 tubes, detection chain and interfaces must respect S4 standards different from the SAT and LAT SO :



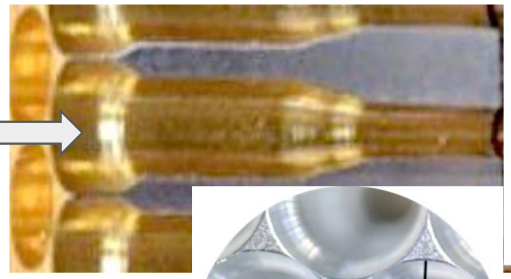
Polarization sensitive & Multi-Chroic concept

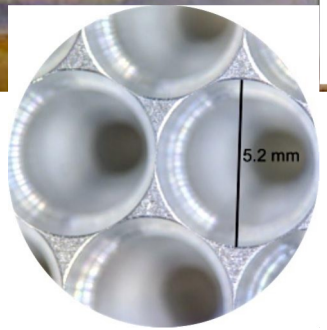


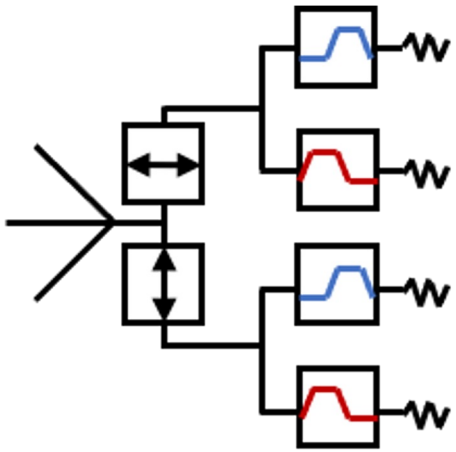
Sky Signal



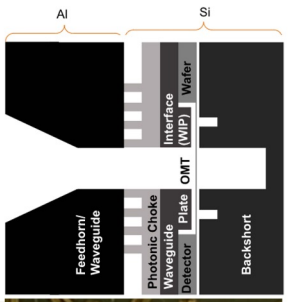
spline-profiled Horn* array



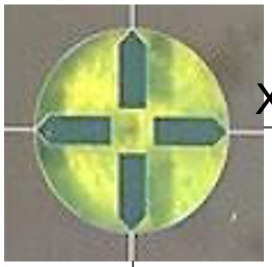




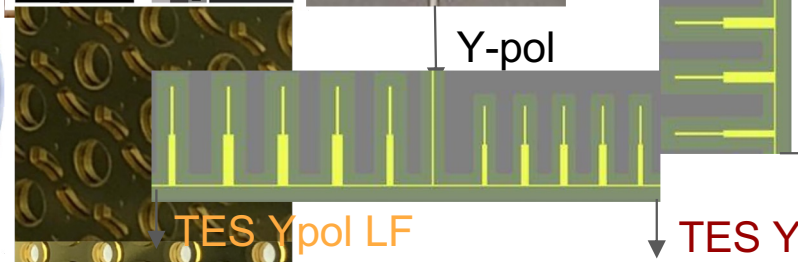
Interfaces layers**



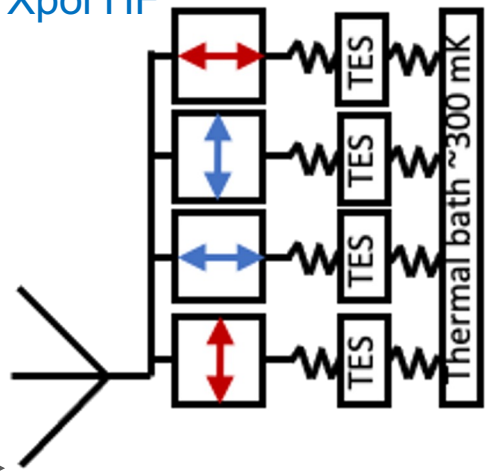
OMT***

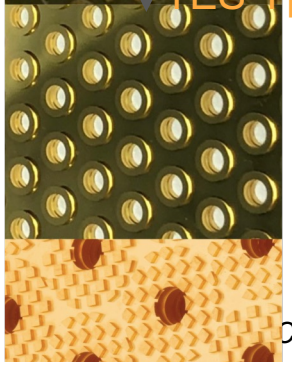


Diplexer****



TES Xpol HF





- Sensitive to **polarisation** antenna
- Superconducting **Channelizer** / Diplexer
- End line **dissipator** + Thermalization
- **Bolometer** + Superconducting thermometer

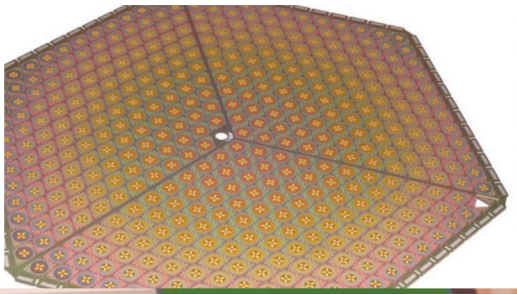
*Feedhorn dev. and scalability for SO and beyond - S. M. Simon et al.
** Conceptual Design …for the CMB-S4 survey experiment, D. Barron et al.
*** JLTP 2022 DOI: 10.1007/s10909-022-02731-x
****Multi-Chroic Detectors for Observing the CMB - A. Traini, M. Piat et al.

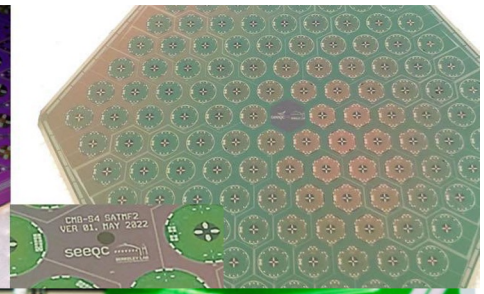
TES : polarisation sensitive + multichroic

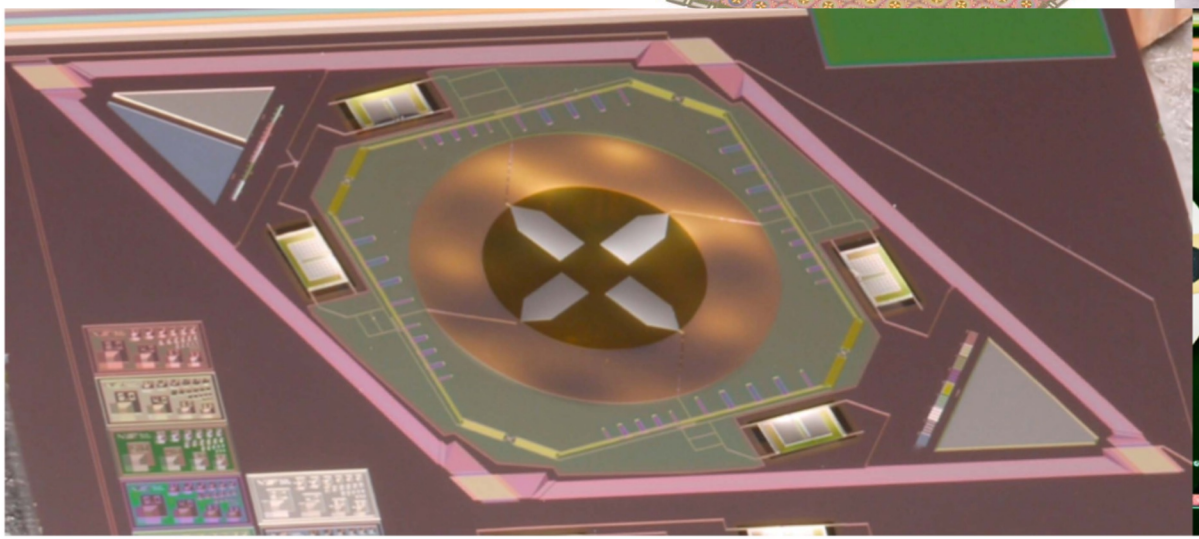
6 fabrication sites : NIST, Argonne, UCB, LBNL/SQC, JPL

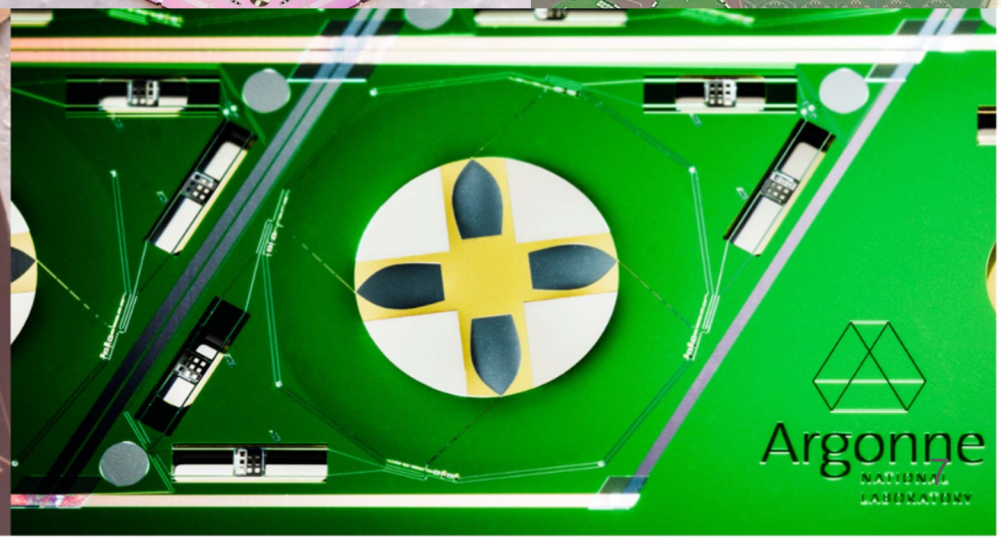
SAT : 30/40 GHz, 85/145 GHz, 95/155 & GHz 225/278 GHz

LAT : 20 GHz, 30/40 GHz, 90/150 GHz & 225/278 GHz

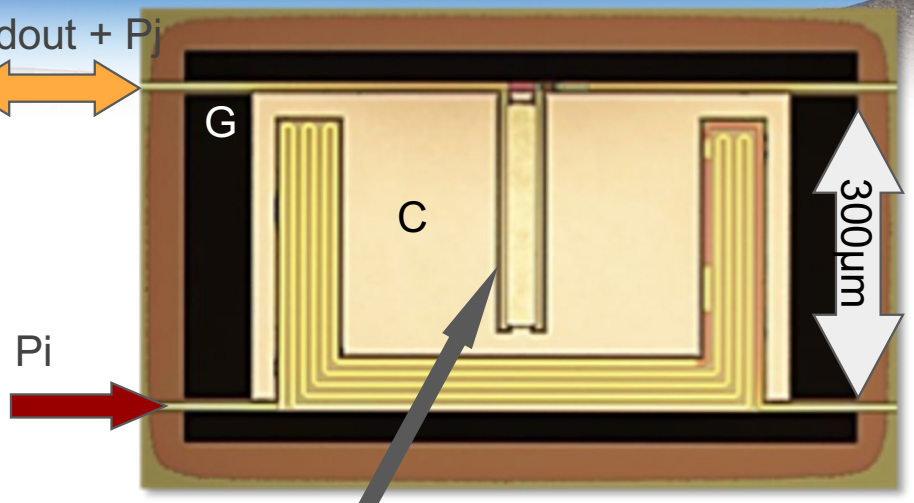








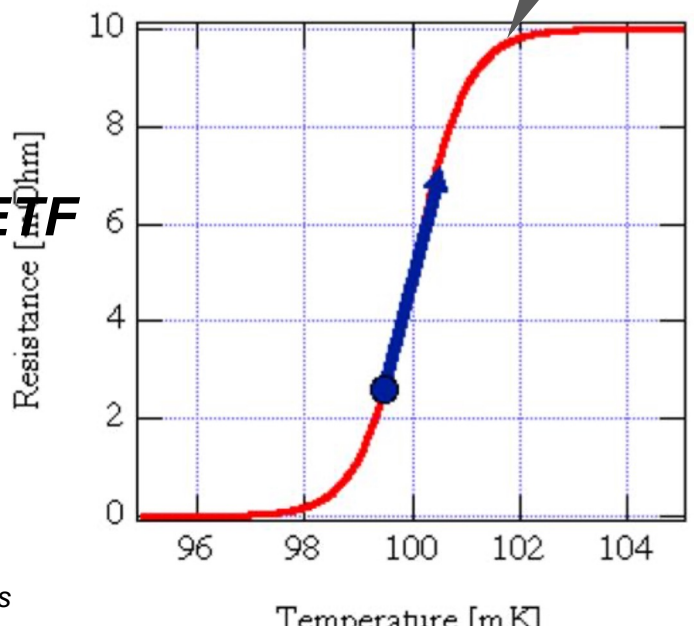
Transition Edge Sensors

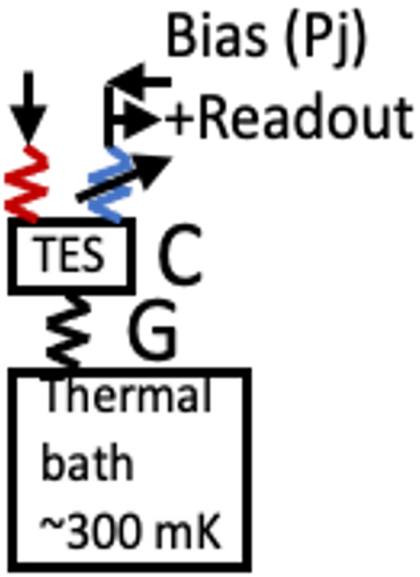


- **Quadratic detection** at the line end
- Bias dissipation ➡ $P_J = V_{bias}^2/R_{TES}$
  - auto **adjustment in an array** @ Tc
  - **response homogenisation response** $\partial I_{TES}/\partial P_J = 1/V_{bias}$
  - Improve time response < C/G

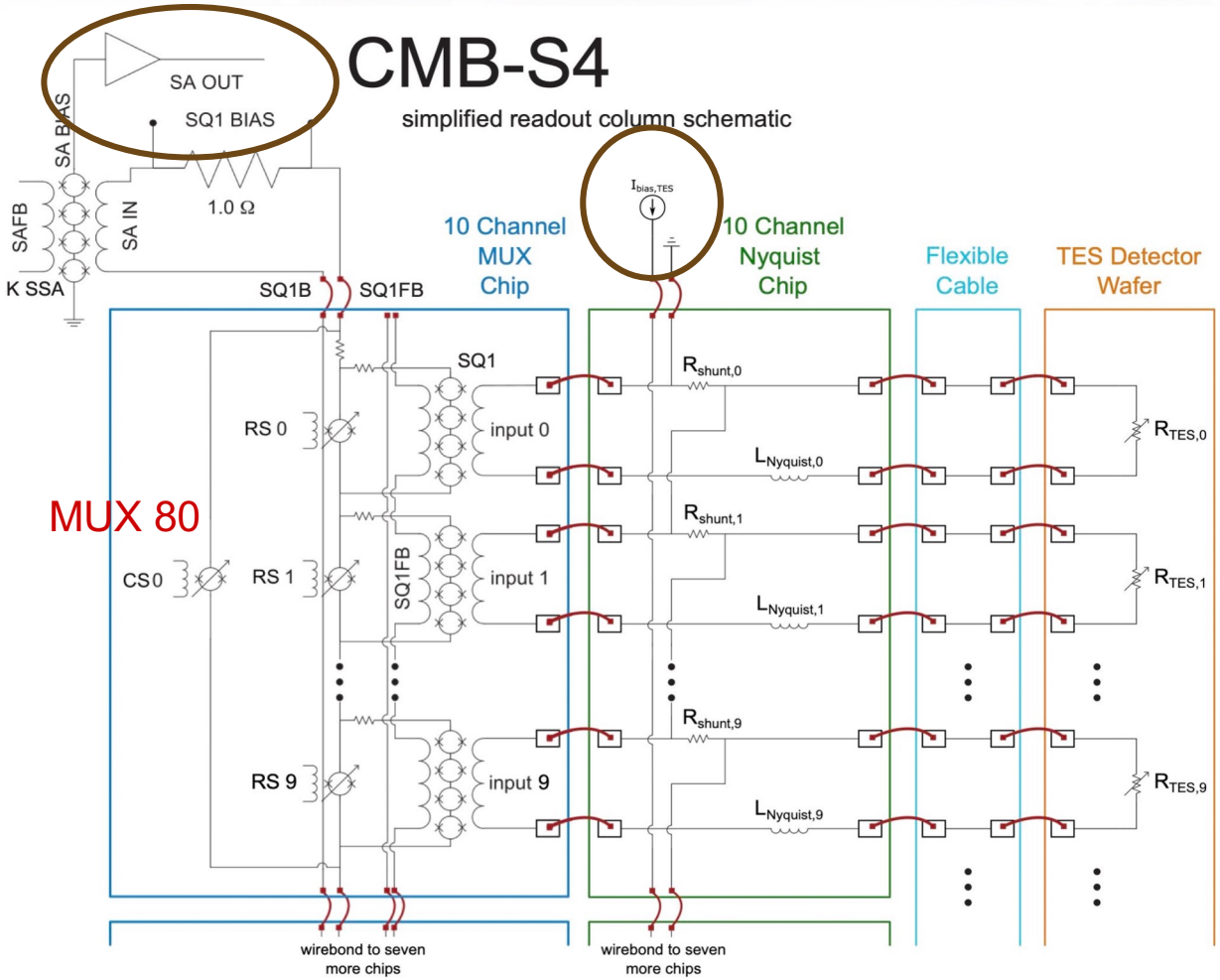
Strong Electro Thermal Feedback - ETF

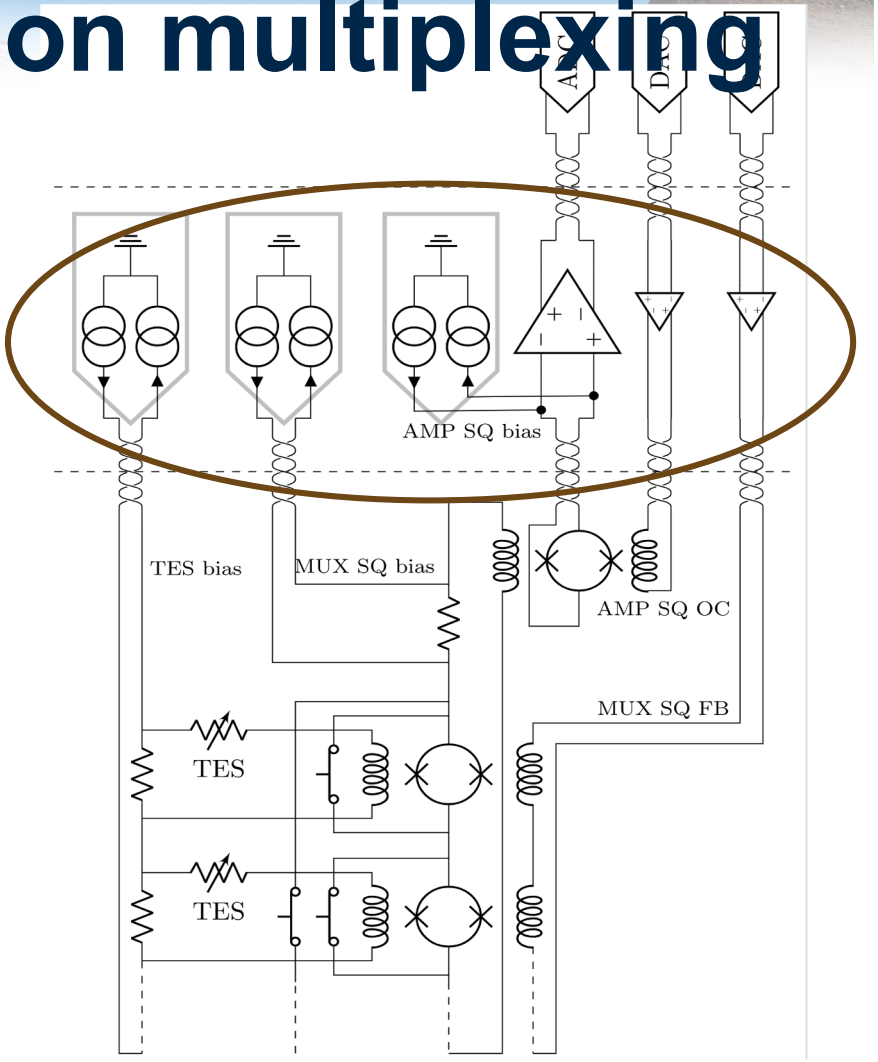
➡ **Voltage biasing**
= detection transfer function



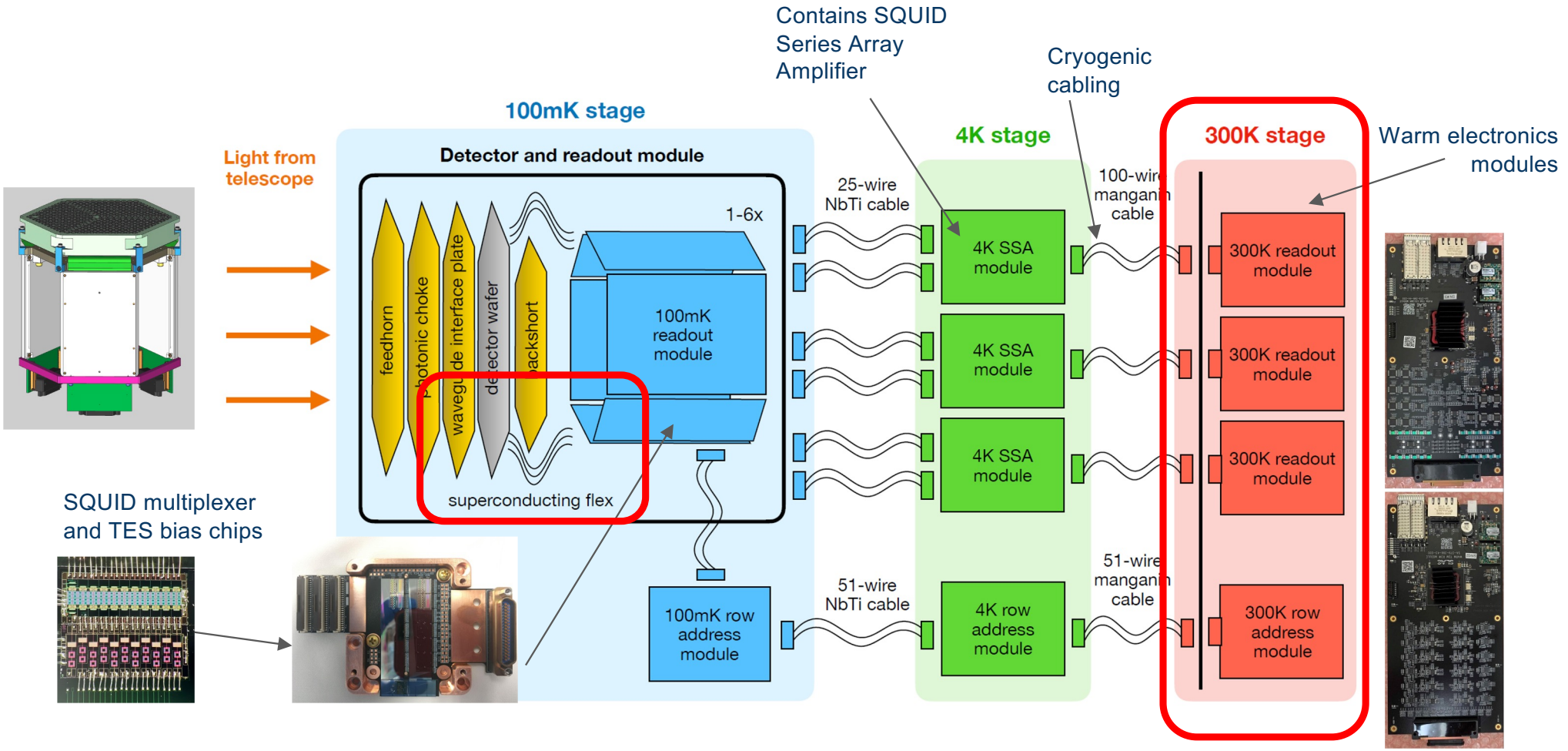


Readout and Time-division multiplexing





Readout subsystem

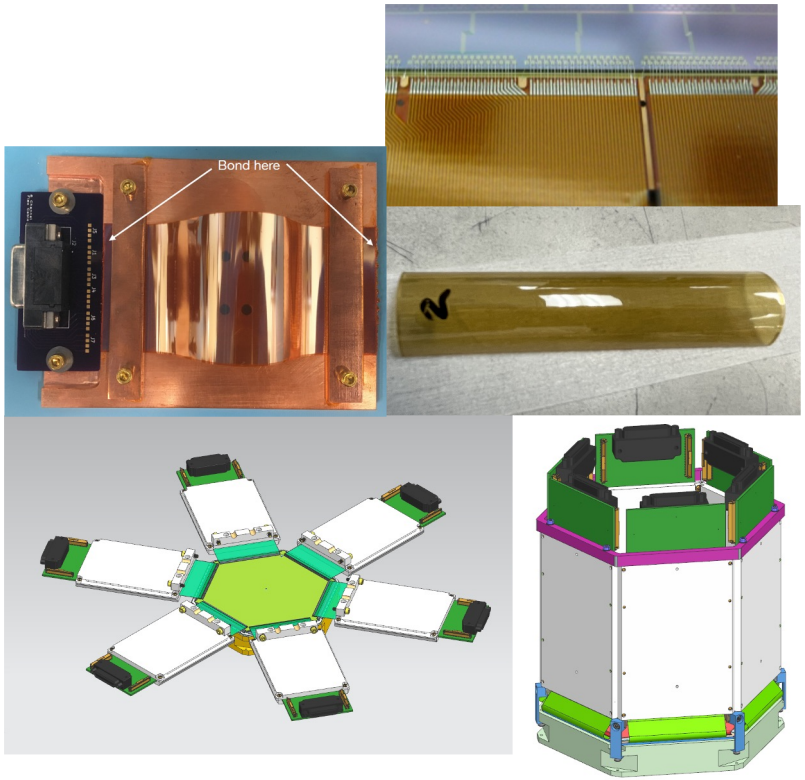


Superconducting Flex

- Development led by CEA
- Production planned to be carried by two companies Hightec and Cicor/Microtech.
- Flexible
- Superconducting
- Low parasitic resistance ($\ll 1 m\Omega$)
- High yield (~100%)

AI assisted **visual inspection** tool to be developed

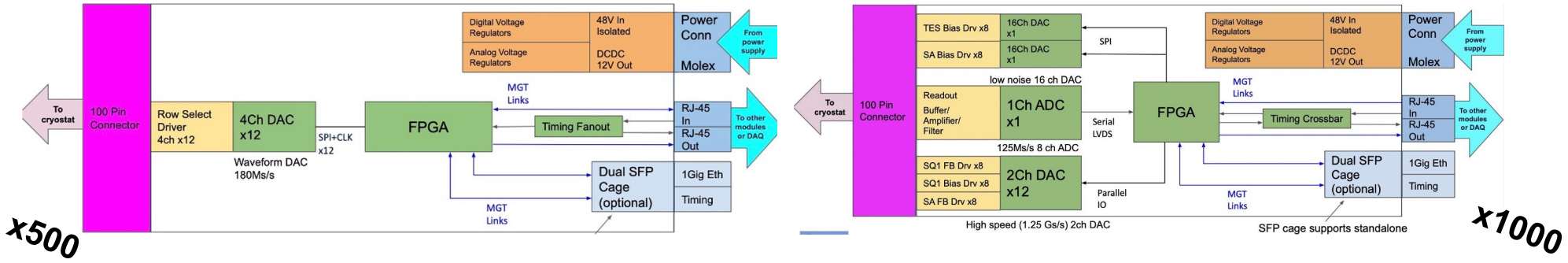
Cryogenic tests to be performed at APC/Cryo-MAT

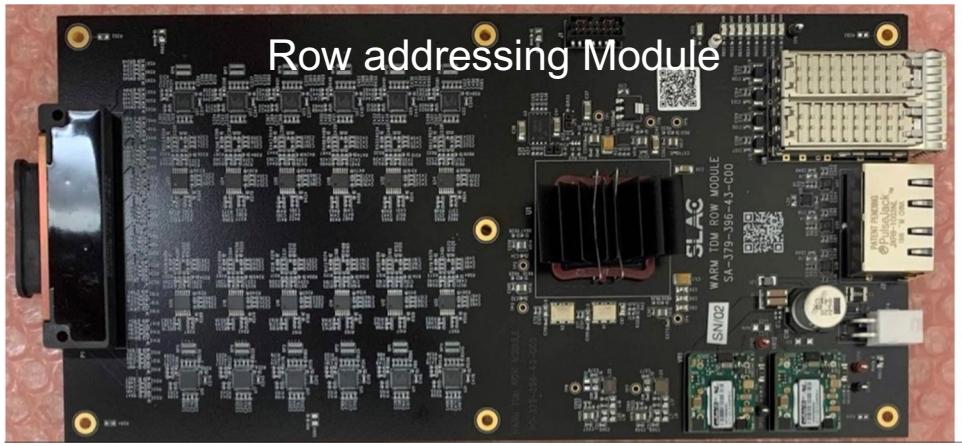


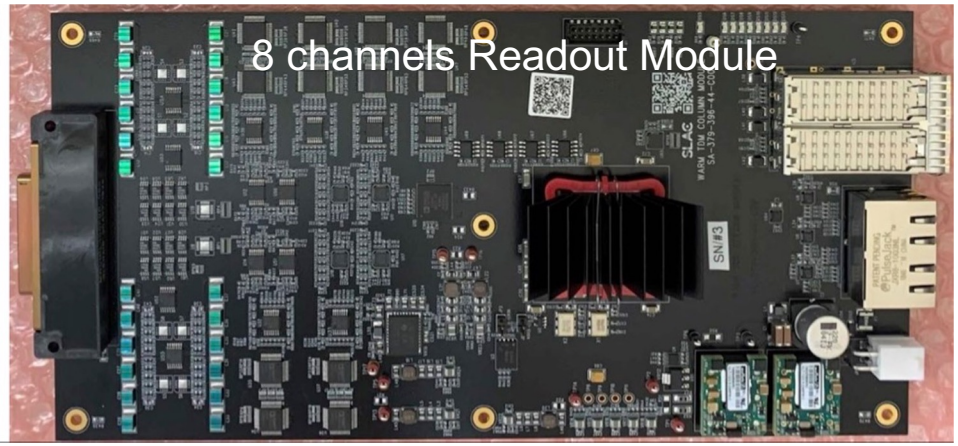
CEA-Irfu: Xavier de la Broïse, Jean-Luc Sauvageot, Jean-Baptiste Melin, Etienne Burtin, Sotiris Loucatos
CNRS-In2p3-APC: Damien Prêle, Manuel Gonzalez, Michel Piat, Jean-Pierre Thermeau

Warm readout

This subsystem is under SLAC responsibility

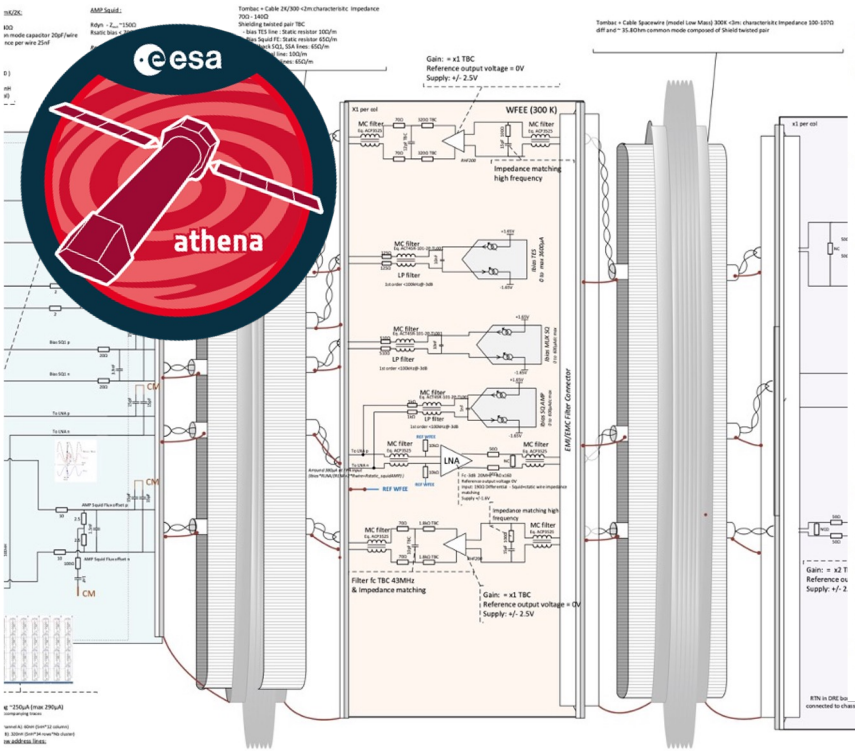






Warm readout background

Front-end readout ASIC family designed for ATHENA X-IFU



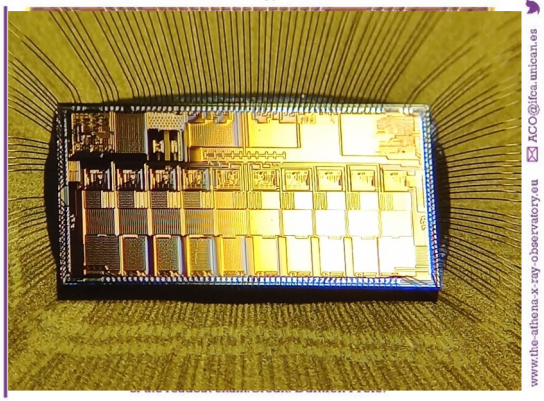
Specific Integrated Circuit for the X-IFU Warm Front-End Electronics

Damien Prêle (APC, Paris) on behalf of the WFEE and X-IFU detection chain team.

The X-IFU (X-ray Integral Field Unit) instrument of the Athena mission is designed to operate with 3168 superconducting microcalorimeters (read out by Transition Edge Sensors - TES) cooled to 50 mK, providing an imaging spectrometer for X-ray astronomy. The unprecedented spectral resolution of 2.5 eV up to 7 keV requires low noise readout electronics. Located immediately outside the cryostat, the Warm Front End Electronics (WFEE) is a key component of the readout electronics.

The WFEE amplifies the detection chain signal, adjusts the operating points of the cryogenic devices (Superconducting QUantum Interference Devices - SQUIDs), and feeds through the TES bias and feedback loop. Using Frequency Domain Multiplexing (FDM, see Athena Nugget #25 for more details), 40 microcalorimeters are read out per channel and 40 carriers between 1 to 5 MHz are injected to 40 sensors. As a result, the detected X-ray pulses are transposed into 40 different frequencies. Ultimately, about one hundred channels are needed for the full readout of the TES array.

To meet the energy resolution of the cryogenic sensors, the WFEE, like the whole readout chain, has to exhibit ultra-low noise and extremely small gain-drift. At the same time, the size, the mass, and the dissipation must be minimized as required for a space mission. For this reason, an Application-Specific Integrated Circuit (ASIC) has been designed for the WFEE. "350 nm BiCMOS SiGe" ASIC technology is used for the core of the WFEE. "350nm" corresponds to the minimum gate size of MOS transistors. "BiCMOS" means that both bipolar transistors and complementary (N and P) MOS transistors can be built using this technology. Finally, "SiGe" indicates that Silicon-Germanium alloy is used to make the base-emitter junction of the bipolar transistor. Such a hetero-junction increases the speed of the transistors allowing the design of a wide-band amplifier covering the frequency range of the carriers used for the FDM. The micro-photograph illustrates an ASIC chip design for the WFEE. Eight independent readout channels will be integrated on a chip of one square centimetre.



The noise degradation of WFEE is minimized by reducing any parasitic resistance and thanks to fine-tuning of the transistors biasing to operate in an optimal noise condition.

The gain drift is also a significant contributor to the energy resolution budget. At large time scale (> 1s), the thermal drift is the main cause of electronic parameter shifts. The entire circuit is based on a specific design including thermal compensation techniques.

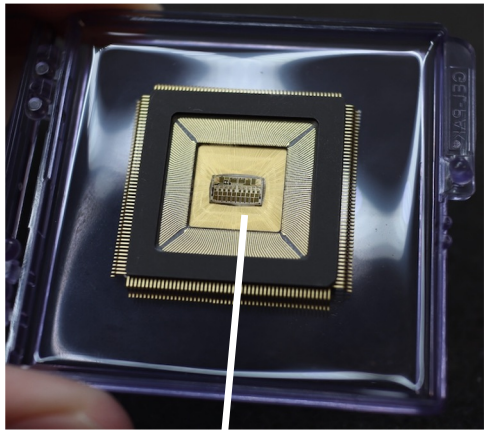
The WFEE with its custom designed ASIC is a compact, light-weight component with minimal power consumption and it delivers the high performance required for Athena's X-IFU readout electronics.

IFU | Project: ATHENA X-IFU | Ed.: DJD 1.2 | Rev.: 0 | Date: 20/04/2022 | Format: custom | Page

Athena X-ray Observatory @AthenaXobs ACO@ifca.unican.es www.the-athena-x-ray-observatory.es

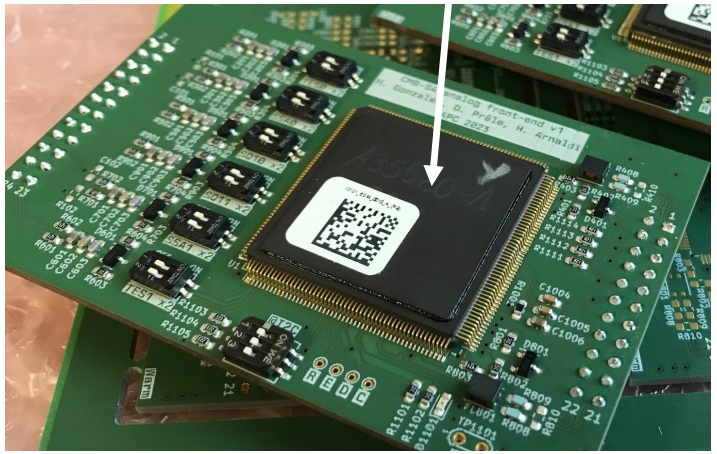
Front-end readout daughter board

Drop-in integrated circuit for analog readout.
Bias and amplification for 2 TDM columns.
Initially developed for X-ray TES readout (ATHENA)
Fully differential, low noise and low thermal drift.



Daughter board based on current package

- Fabricated
- **Delivered last week**
- First tests/adjustments currently done



2 x **LNA** 20 MHz 0.7 nV/√Hz
2 x DC DAC for **SQ1 bias**
2 x DC DAC for **SSA bias**
2 x DC DAC for **TES bias**
DACs controlled through I2C

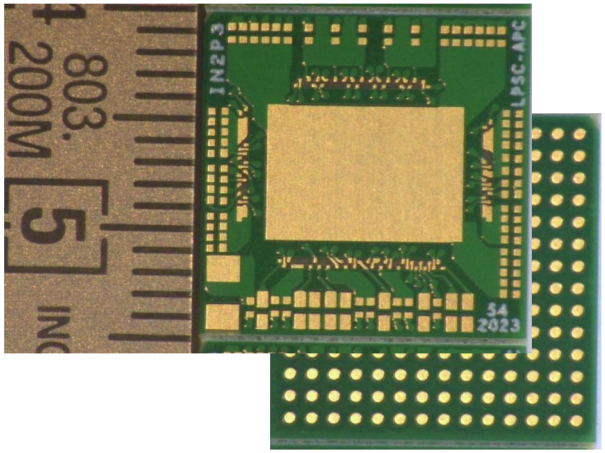
Design of new compact BGA package

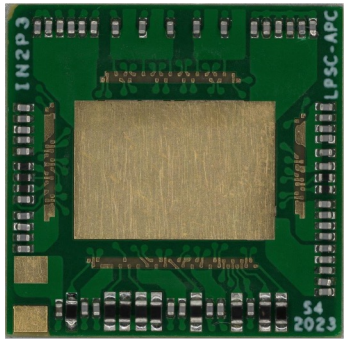
1.5 cm PCB with glued and bonded ASIC naked die and passive components
Compact system in package of the ASIC as a BGA*
In preparation for 4 ASICs integration in one board

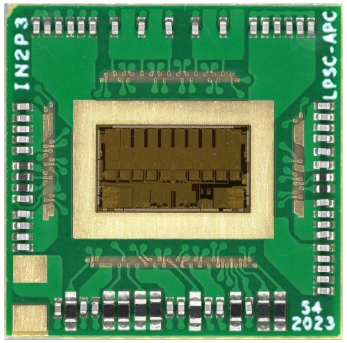
*Ball Grid Array - BGA : chip carrier, surface-mount packaging

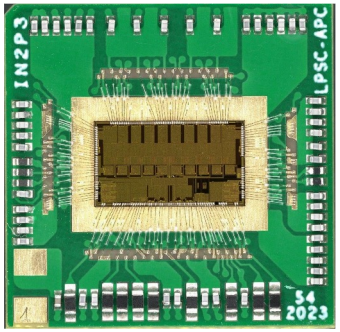
Company	Work	Delay
PCB electronics (french company)	**PCB Fabrication**	4 weeks
LPC Clermont-Ferrand (IN2P3 Lab)	**Soldering** - Passive components	2 weeks
C4PI @IPHC (IN2P3 Lab)	**wire bonding** - Chip on Board	2 weeks
Itancia	Solder Bump	6 weeks

WE ARE HERE

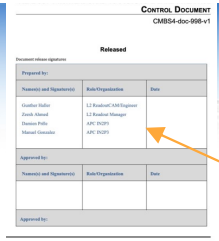








CMB-S4 Task Order / IN2P3 - CRADA


CONTROL DOCUMENT
CMBS4-doc-998-v1
Released

- Objectives identified in a CRADA
- Real ongoing collaboration with SLAC
- First hardware produced in December 2023

B. Design, development, and deployment of components an management subsystem WBS 1.09:
- 1.09.02 Data Movement. Design, development, d operation of:
  - Data registration system
  - Data archiving system
  - Data distribution system (specifically in distribution center is included in the pro
- 1.09.03 Software Infrastructure
  - Data Model: DD&D of a metadata inte
  - Software Deployment: system-specific workflows (specifically in the event th is included in the project scope)
  - Workflow Execution: execution of da
- 1.09.04 Data Simulations. DD&D of:
  - Software modules to simulate syste
  - Software modules to simulate syste
  - Validation & Verification systems
- 1.09.05 Data Reduction. DD&D of:
  - Systems to characterize the instru systematic effects) from the raw a
  - Software modules to mitigate sy time-ordered data to well-charac
  - Validation & Verification system

TECHNICAL OBJECTIVES
The Parties intend to collaborate to develop designs systems to validate conceptual and preliminary desi

ANNEX B
CMB-S4 Task Order
(HEREINAFTER "Project")

October 2023

This Task Order is subject to and governed by CRADA No. FP00006410 ("CRADA") between the Parties and all the terms, conditions, definitions, and provisions of said CRADA are hereby incorporated by reference. The Parties agree to perform their respective obligations related to this Project in accordance with the terms and conditions of this Task Order, Annex A (Master SOW) and other documents attached or Incorporated by reference, which together constitute the entire Task Order. In the event of any conflict between the provisions of this Task Order and the provisions of the CRADA, the CRADA shall control.

HOME INSTITUTION: IN2P3
HOST INSTITUTION: LBNL, as lead laboratory for the CMB-S4 Project.

PROJECT DESCRIPTION: Cosmic Microwave Background – Stage 4 (CMB-S4) Project

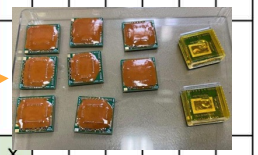
BACKGROUND
The Parties intend to work jointly toward fabricating and operating an instrument capable of meeting the CMB-S4 scientific requirements by participating in scientific and technical collaboration in the field of cosmic microwave background physics in support of the CMB-S4 Project areas. This Annex outlines the proposed collaboration between LBNL, as the lead laboratory for the CMB-S4 Project, and IN2P3. Work under this agreement may include visits and assignments to other U.S. institutions within the CMB-S4 Project, coordinated through LBNL.

ESTIMATED PERIOD OF PERFORMANCE
The estimated Period of Performance of this Task Order is from October 1 2023, through September 30 2026. It is intended that joint work during the Project construction phase will be further clarified as the Project Performance Baseline is develop

	Task/Milestone	Work Done By		Execution Period to Completion Quarters After Start start in October 1, 2023											
		CMB-S4	IN2P3	1	2	3	4	5	6	7	8	9	10	11	12
R0-01	ICD for ASICv3 2-channel integration with CMB-S4 front-end module for warm readout module	X	X	X											
R0-02	Design/fab/bench-test ASIC daughter board with one ASICv3 (2 channels) in a CQFP208		X		X	X									
R0-03	Modification (design/fab/bench-test) Front-End Board to accept ASICv3 daughterboard	X				X	X								
RO-04	Performance testing and analysis of results for v3 in CQFP208 package on front-end module.	X					X	X							
R0-05	Package 2-channel ASICv3 in a new smaller chip package. Update ASIC daughter board.		X		X	X	X	X							
R0-06	Performance testing and analysis of results for 2-channel v3 in new smaller chip package on front-end module.	X						X	X						
R0-07	ICD for vS4 ASIC chip integration with CMB-S4 warm readout module	X	X					X							
R0-08	Design, DOE/IN2P3 review, fab of ASICvS4 chips, supporting daughter boards, pre-test		X						X	X	X	X	X		
R0-09	Modification of warm readout module to accept ASICvS4	X										X	X	X	
	daughter board														
R0-10	Performance testing and analysis for vS4	X												X	X

in preparation

soon



Conclusions and way forward

- Strong **interest** of the CMB community on the CMB-S4 science and instrumental developments
- Readout contributions/activities for the **next three years formalized**
- **Cohesive effort to capitalize** the development for other CMB projects
- Strong **collaboration with SLAC**
- **First French CMB-S4 hardware delivered last week**
- We need to **start thinking about the production phase**