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An ASIC for Real Time Analog Pulse Shape Discrimination

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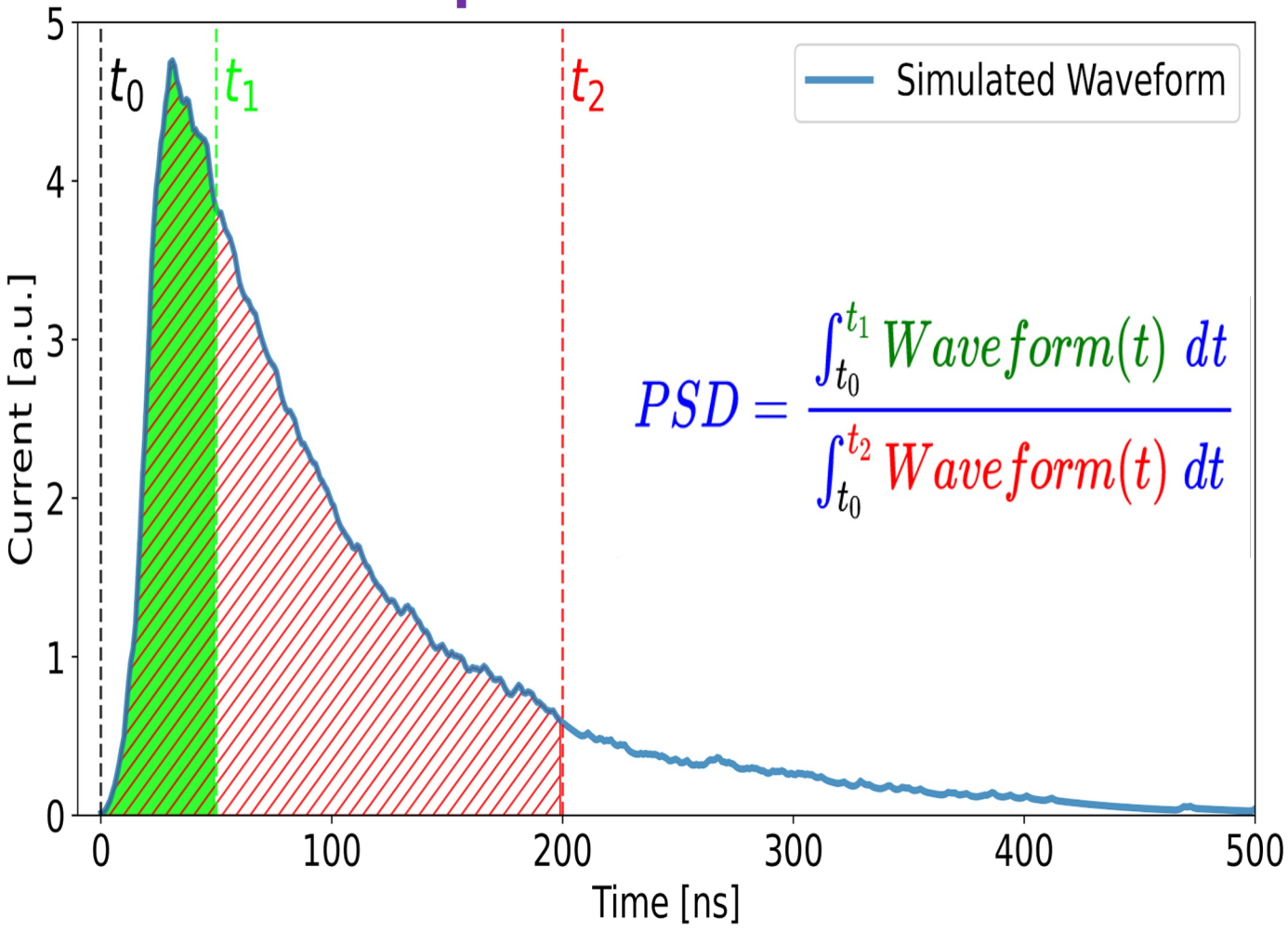
Reminder: Pulse Shape Discrimination

- Emission spectra can be dependent on the type of interacting particle, especially due to differential excitations of various excited states, which subsequently decay with distinct decay constants.
- The resultant electronic signal pulse has these characteristics encoded in its temporal profile.



We are defining and implementing an electronic version of this concept on a custom chip (PSD_ASIC) that discriminates between neutrons and gammas based on the quantity PSD, as defined above.

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Why analog PSD?

An ASIC capable of discriminating particles by their induced pulse shape (PSD) in real time will enable various implementations.

Current schemes mostly involve digitizing the pulse and performing PSD on the digitized data. This method consumes substantial power and has a high per channel cost.

An ASIC with analog PSD capability will comsume much less power, will have a low per channel cost when mass produced, and will eventually be cryogenic compatible.

Nuclear Non-proliferation Monitoring is a high priority item, and novel neutron detection systems are being continuously developed. Such an ASIC could serve as the critical front-end of a sensor array or be an important component in a larger readout system.

Liquid Argon has a pronounced PSD signature, which has been fully exploited in Dark Matter searches. Our ASIC could find use in Lar based detectors, once it has been made cryogenic compatible. Our collaborator, the ASIC design group at LBNL has this expertise.

Neutron radiography is another important area. Current approaches are not fully digital. Our ASIC provides the capability for fast turn-around and real time analysis.

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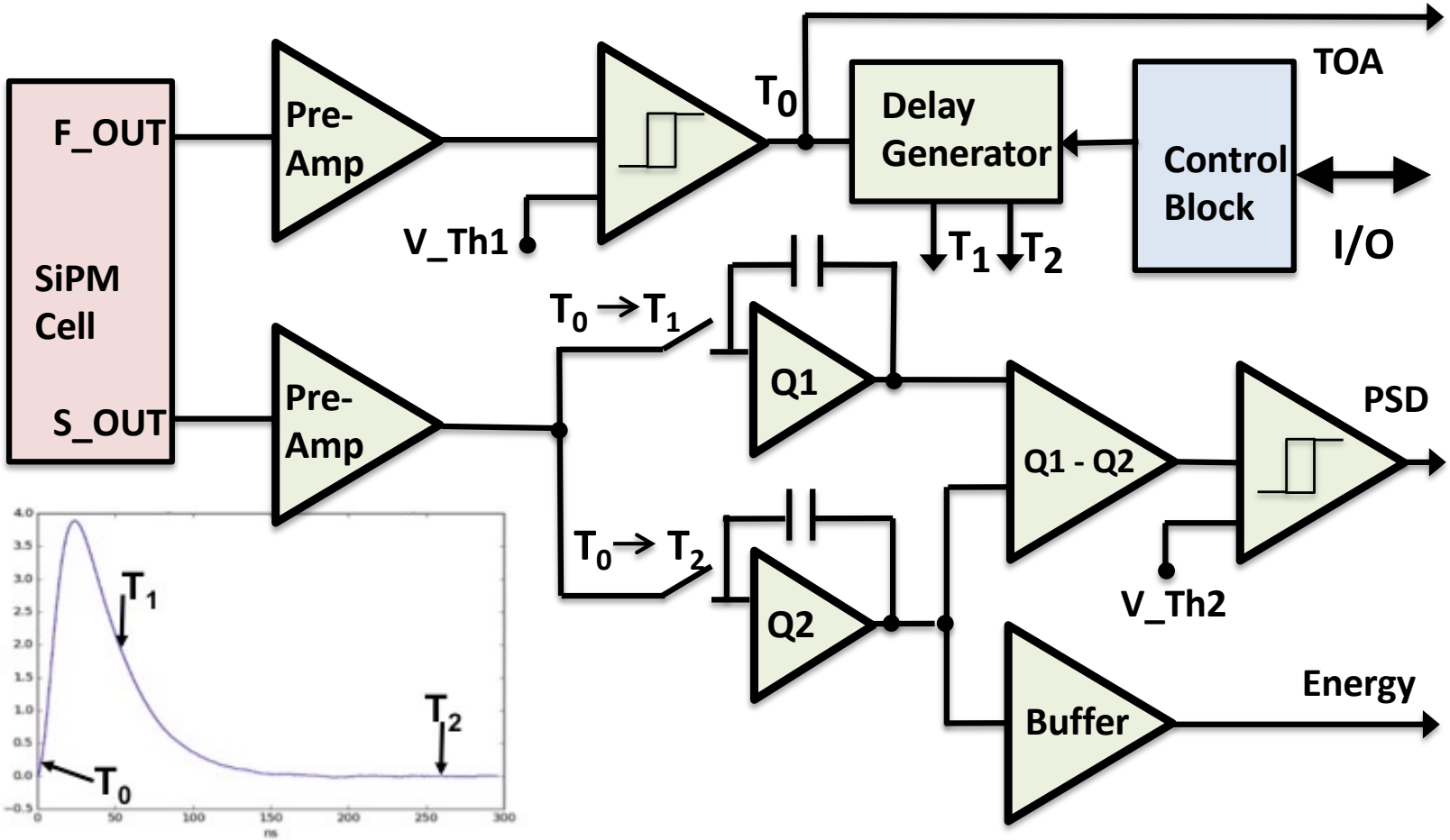
ASIC: Conceptual One Channel Diagram

SensL SiPMs provide a capacitively coupled fast output (FOUT)
and a resistively coupled standard output (SOUT)

ASIC outputs:



a) Fast time of arrival pulse.

b) PSD classification bit

c) Total energy

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Initial Project Goals

- Develop a demonstration ASIC for testing with SiPMs coupled to plastic/organic scintillator materials. Proceeded on two fronts:

  a) Work with digitizers and implement the ASIC's core functionality in analysis software for a design validation study.

  b) Fabricate ASICs in shared wafer runs (180 nm TSMC)

- Software version of the ASIC scheme was applied to digitized data collected from a Scintillator + SiPM Characterization Test Bed, which was exposed to neutron and gamma sources.

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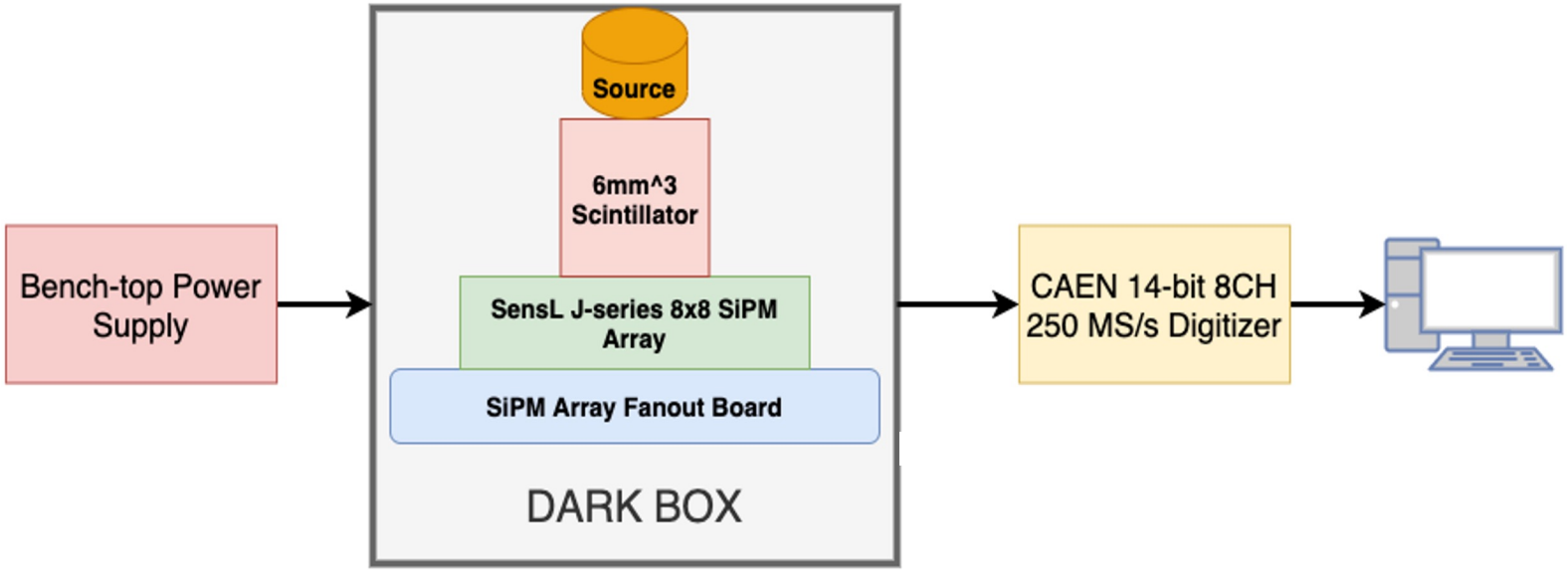
SiPM + Scintillator Characterization Test Bed



- A 6x6x6 mm^3 block of scintillator is coupled to a 6x6 mm^2 SensL J-Series SiPM.
- Both SOUT and FOUT outputs are recorded by a CAEN digitizer (250 Msps)
- Two types of scintillators used: Stilbene and EJ-276.

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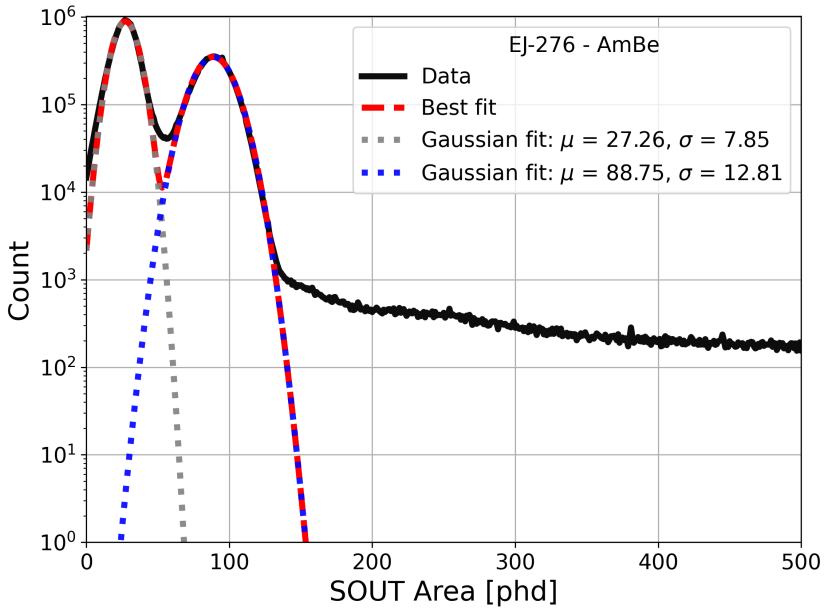
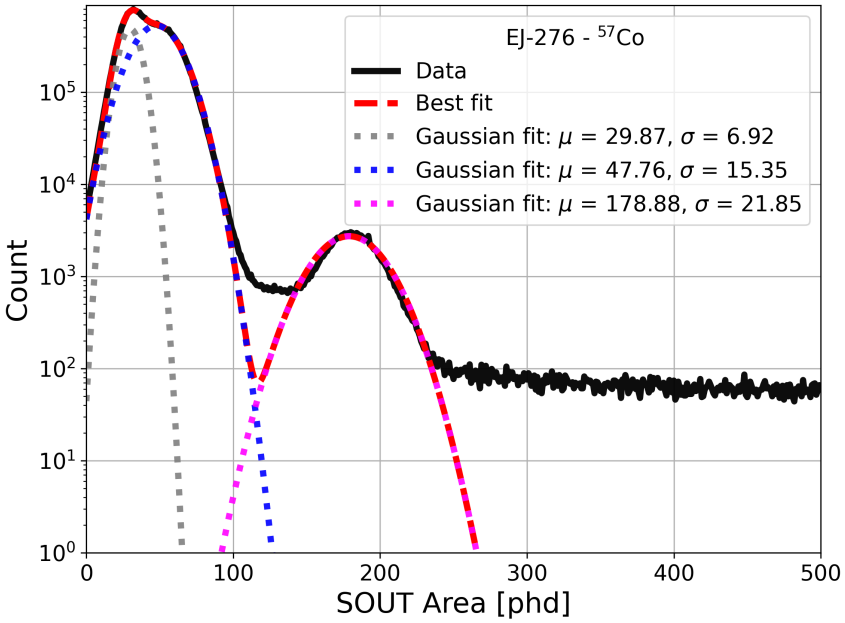
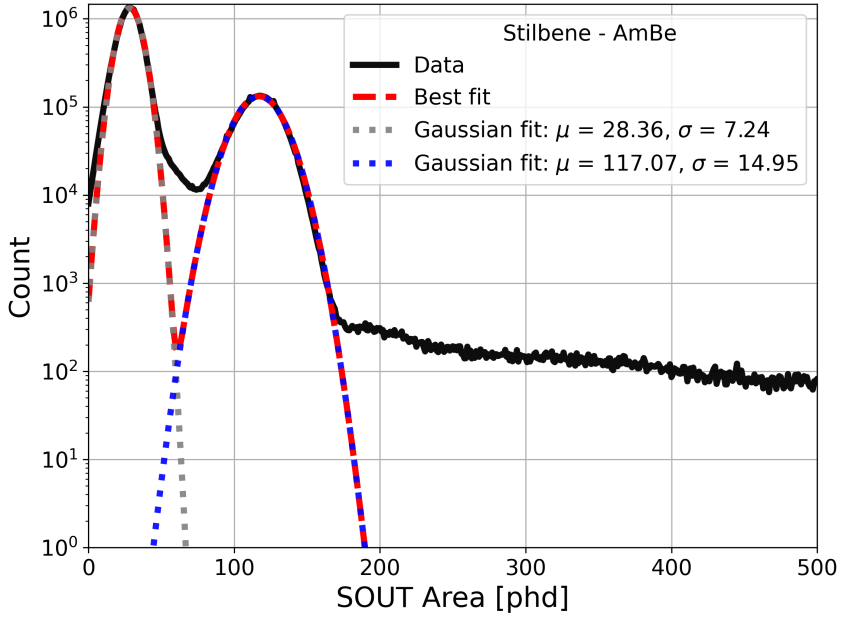
Energy Calibrations with Gamma Sources

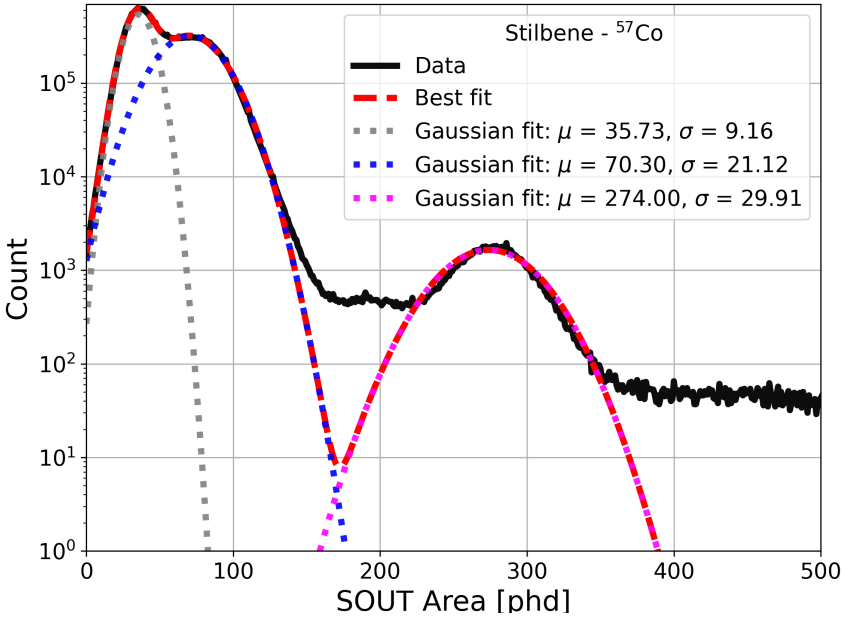


EJ-276





Stilbene



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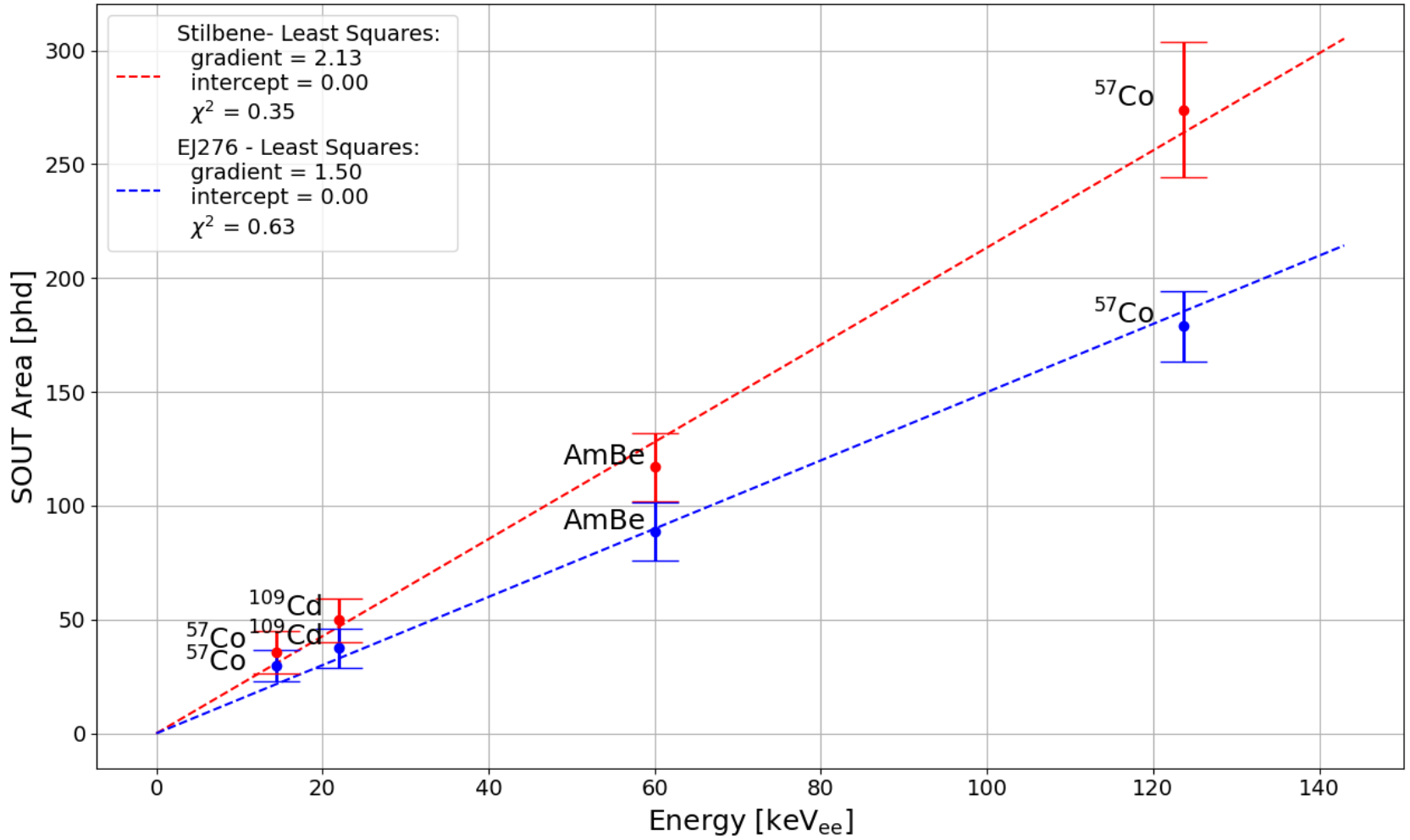
The Response is Quite Linear



As expected, Stilbene (2.13 phd/keV) is brighter than EJ-276 (1.5 phd/keV).

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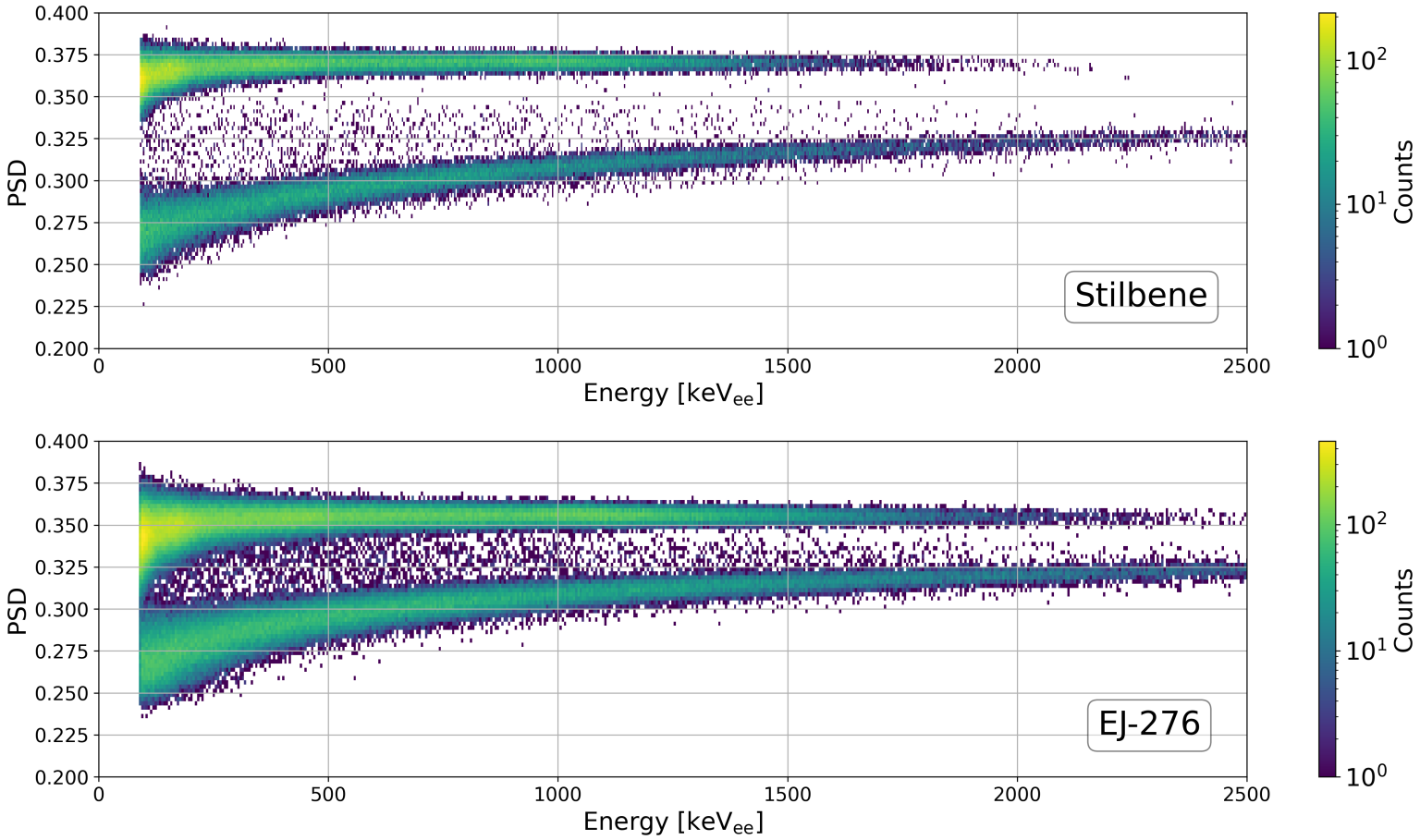
Example of PSD capability

- Dataset consists of 130k (Stilbene) and 280k (EJ-276) AmBe events.
- Good separation down to 100 keV is visible. EJ276 does not do well below ~100 keV.
- Of course, it depends on the light collection efficiency of a particular design.



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PSD_CHIP Design Features

- Real-time tagging of neutrons against gamma background → Analog PSD circuit implemented on chip and verified with play-back data.
- Dual input polarity capable SOUT front end (with programmable TIA gain of x30 – x180)
- Adaptable PSD for different target materials → Programmability provided on chip for selection of short and long integration windows, as per material properties. Fine tuning of total integration windows up to ~2.5us and partial ones up to ~200ns is provided within those dynamic ranges.
- Two methods of generating the partial, total, and hold line delays are implemented on chip → The starved invertor implementation is proven, however, the ramp generator technique promises to be less power hungry. They will be compared for performance on chip.
- FOUT front end is expected to provide rise times <1ns on chip → This verification will need equipment capable of making such measurements.
- Maximum Diagnostics → In the chip design for this prototype, all important nodes are available as external outputs for inspection.
- Front-end system is designed primarily for SensL SiPMs. However, simple off-chip adaption is possible for use with other sensors such as PMTs, MCPs, and LAPPDs etc.

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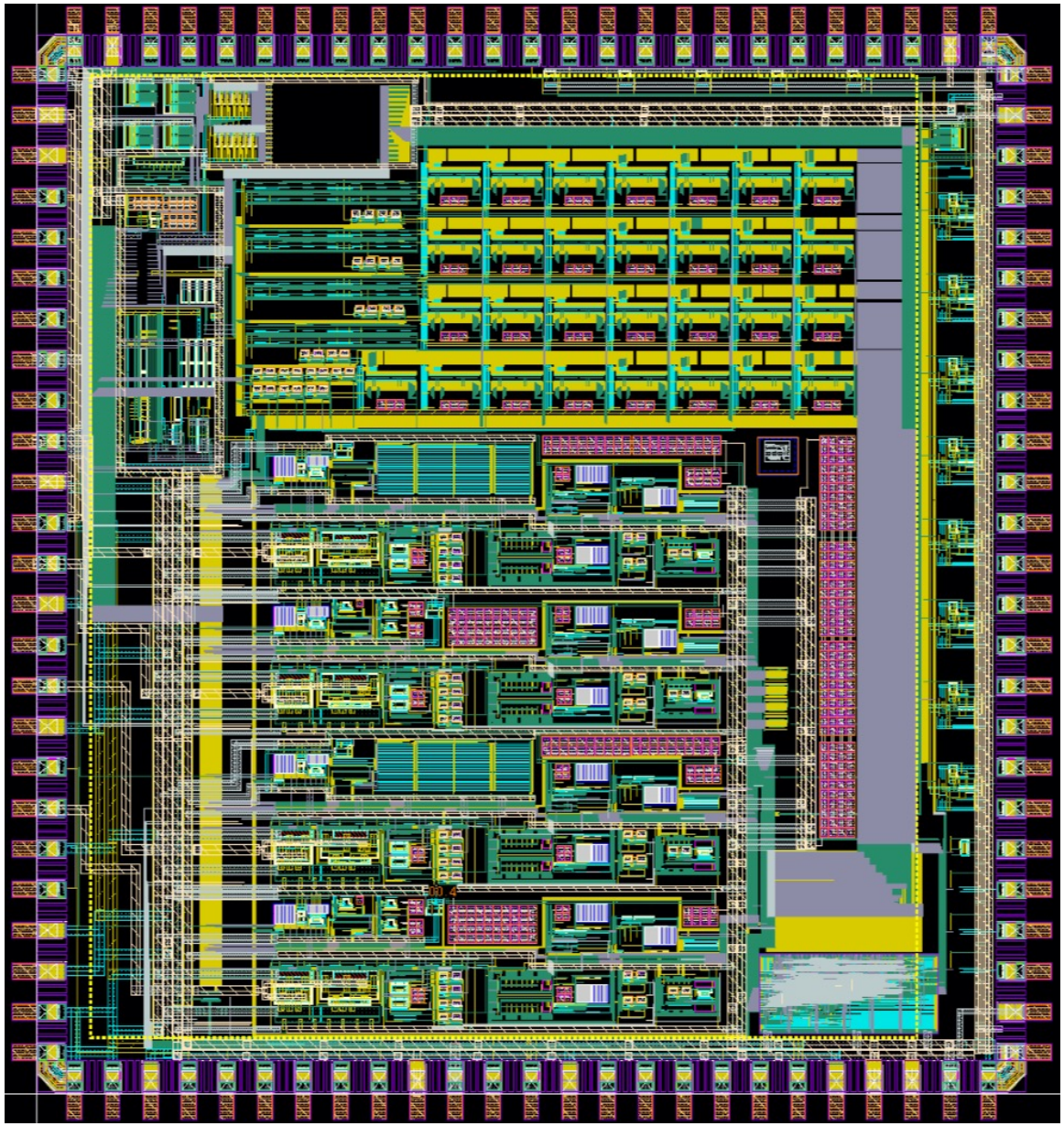
PSD_CHIP V2 Layout Capture

- A prototype 4- channel ASIC has been designed and fabricated in the 180 nm TSMC process.
- It has seen two rounds of fabrication, as is quite customary.
- Testing of v1 informed improvements in v2.
- PSD_v2 chip test setup has been designed and fabricated.
- Bench testing proceeding as of now.



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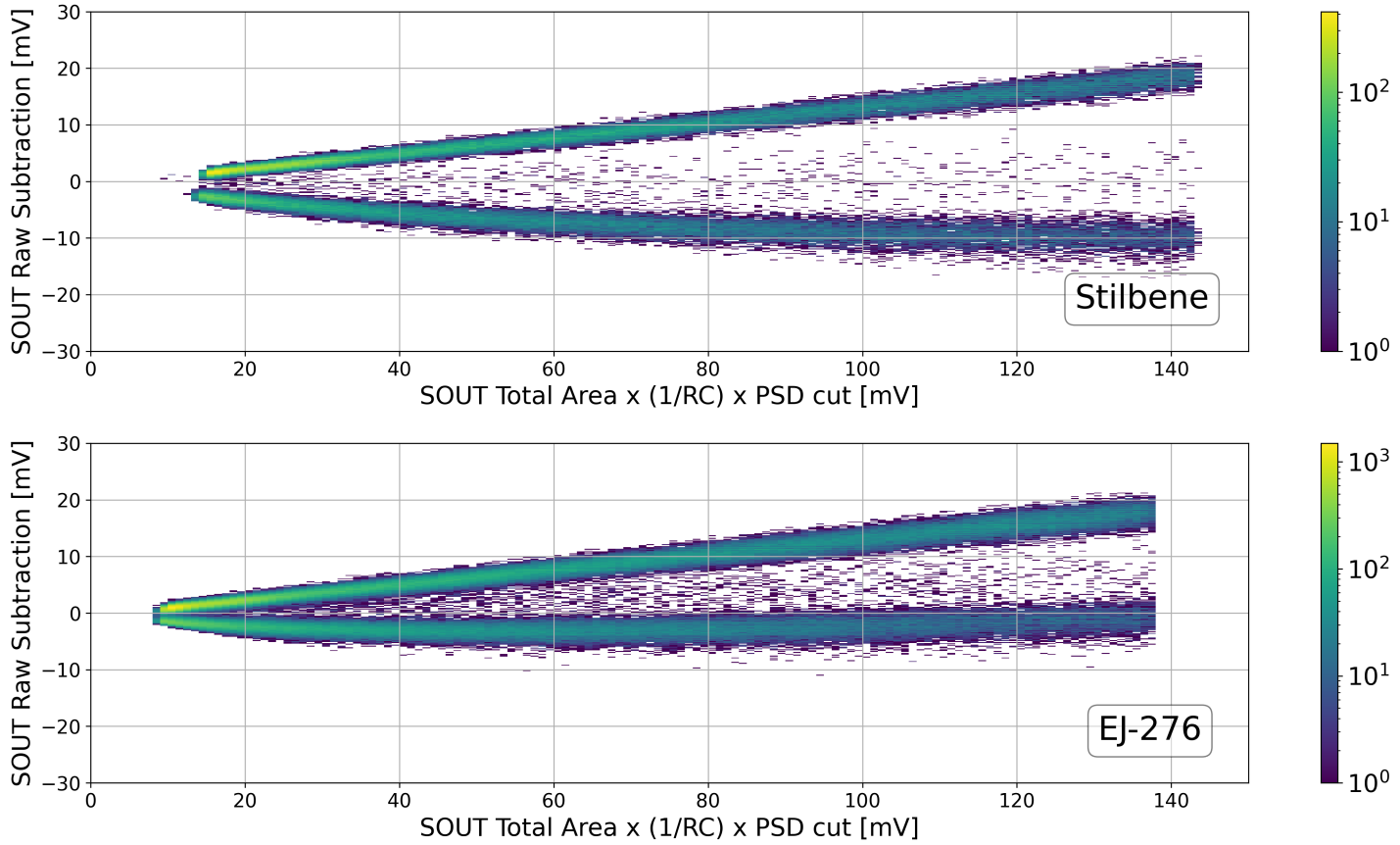
Real-Time PSD Subtraction Space



- By tuning the gain of the total integration, the “cut” in PSD space can be translated into a null difference. Hence, the “threshold” becomes zero.
- Unlike in PSD space, band widths get narrower at lower energies

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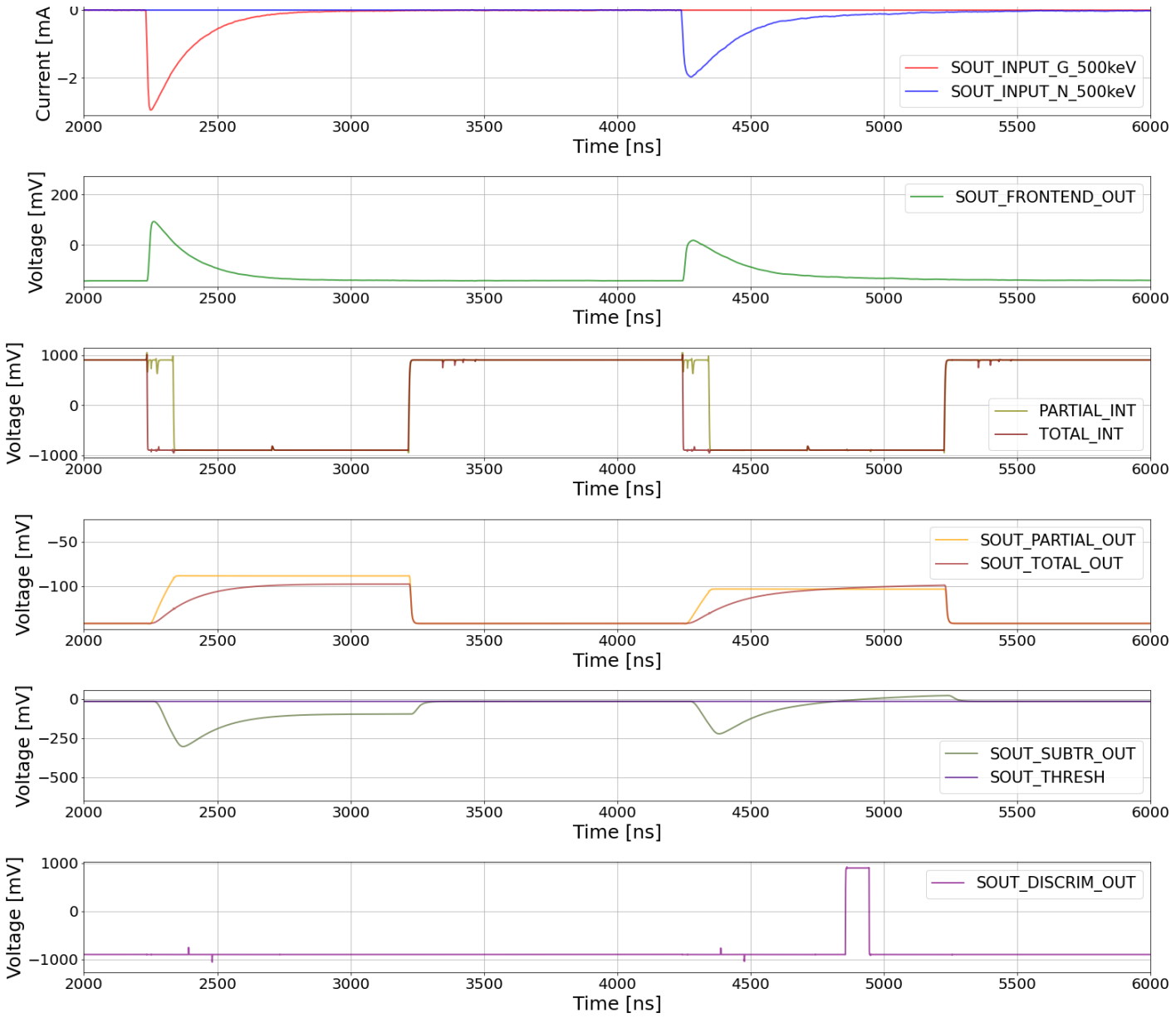
Full SOUT Signal Chain



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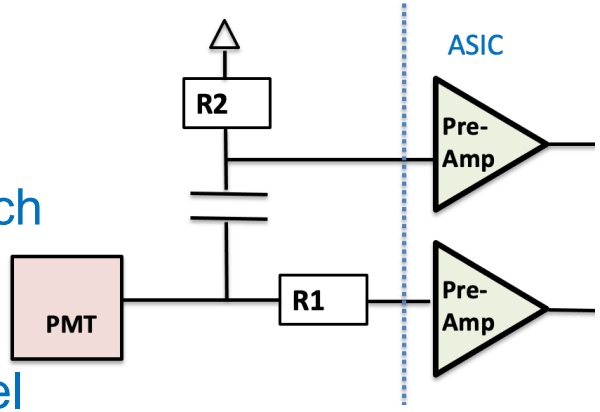
Conclusions

- A 4-channel ASIC has been developed for performing real-time analog PSD.
- Current design is focused on SiPM readout.
- The ASIC can be used with single output sensors such as PMTs.
- The next step will be to proceed to a 32 or 64 channel version. This will involve transporting the design from 180 nm to a 65 nm process.
- Some modifications will be needed to make it functional at LAr temperatures, while consuming less power.
- Results from testing PSD_v2 chip expected soon.



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