ToRA ASIC for the AMBER MM experiment

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AMBER collaboration

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ToRA ASIC project

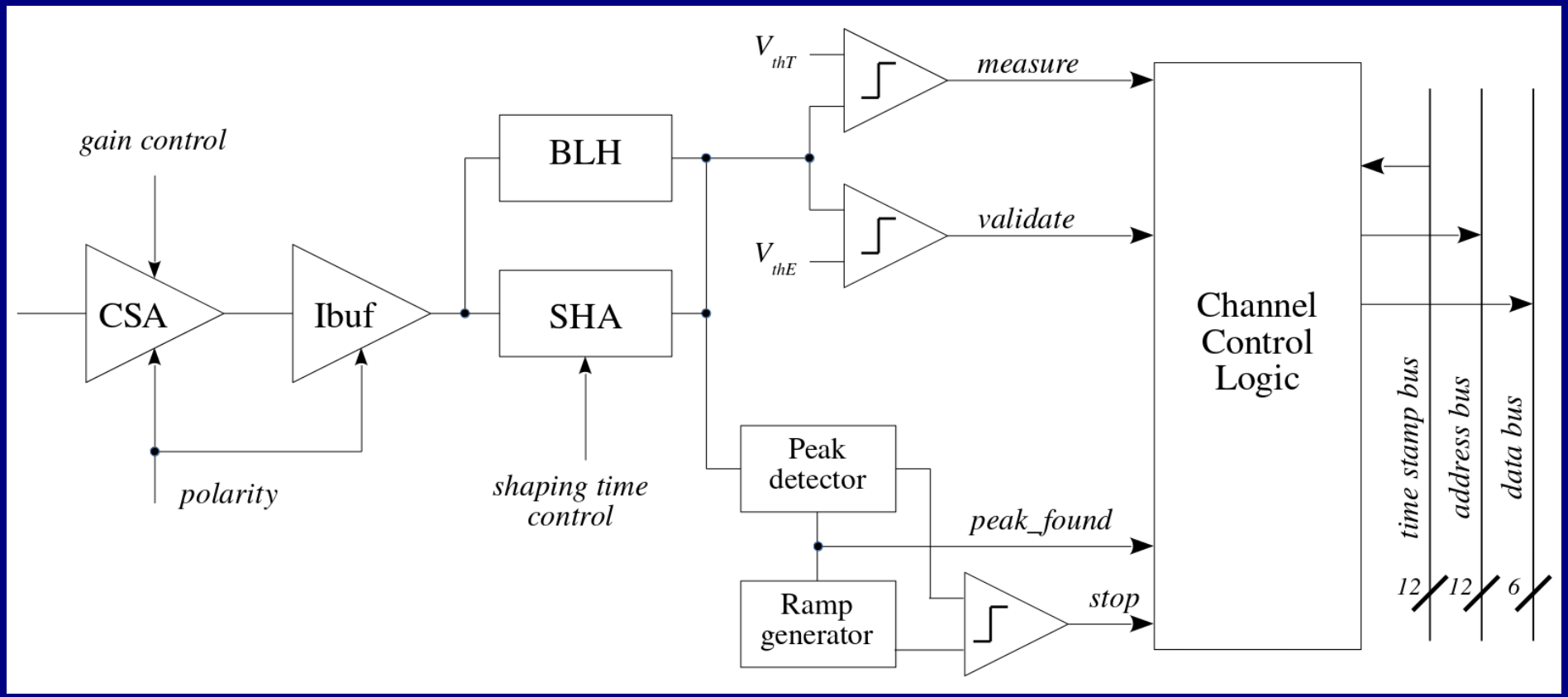
- New development for the MicroMegas detector of the AMBER experiment
- Possibly compatible also with straw detectors
- Moderate timing resolution (1-2 ns or better)
- Analog Front-End : custom development
  - inspired to VMM[(1)] and Tiger[(2)] designs
- Back-end : same as the ToASt ASIC[(3)]
  - silicon proven
  - save time in terms of design and test set-up development

(1) *G.De Geronimo et al.*, The VMM3a ASIC,
IEEE Trans. Nucl. Sci., vol. 69, no. 4, Apr. 2022
(2) *A.Rivetti et al.*, TIGER: A front-end ASIC for timing and energy measurements with radiation detectors,
Nucl. Instrum. Meth., A 924, pp. 181-186, 2016
(3) *G.Mazza et al.*, A 64 channels ASIC for the readout of the silicon strip detectors of the PANDA micro-vertex detector,
J. Instrum., vol. 18, C01020, Jan. 2023

Specifications

Detector	MM	Straw	
Channels/ASIC	64	64	
Power/channel	$\leq$10	$\leq$10	mW
Input capacitance	$\leq$500	20-100	pF
Input charge	1-100	1-1000	fC
Input impedance	$\leq$50 Ω	*tbd*	Ω
Max rate	$\leq$2	$\leq$0.18	MHz
Peaking time	150	75-150	ns
Time resolution	1-2	$\leq$1	ns
Charge resolution	8	10	bits
Gain	12	2	mV/fC
ENC @10 pF	500-1000		e^-
ENC @150 pF	1000-2000		e^-
ENC @60 pF		3000	e^-
Threshold range	*tbd*	0-15	fC
Clock frequency	200	200	MHz

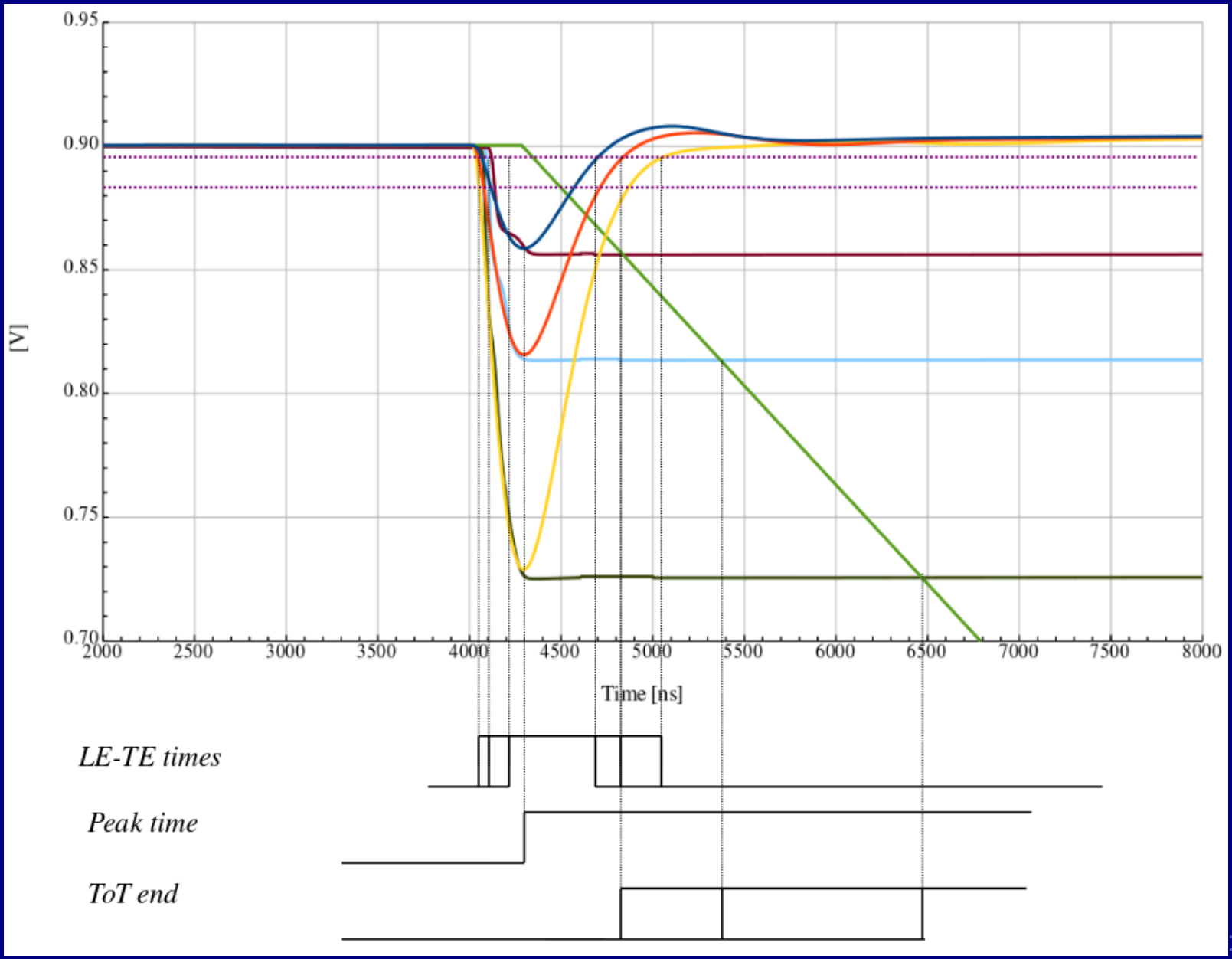
Analog channel architecture



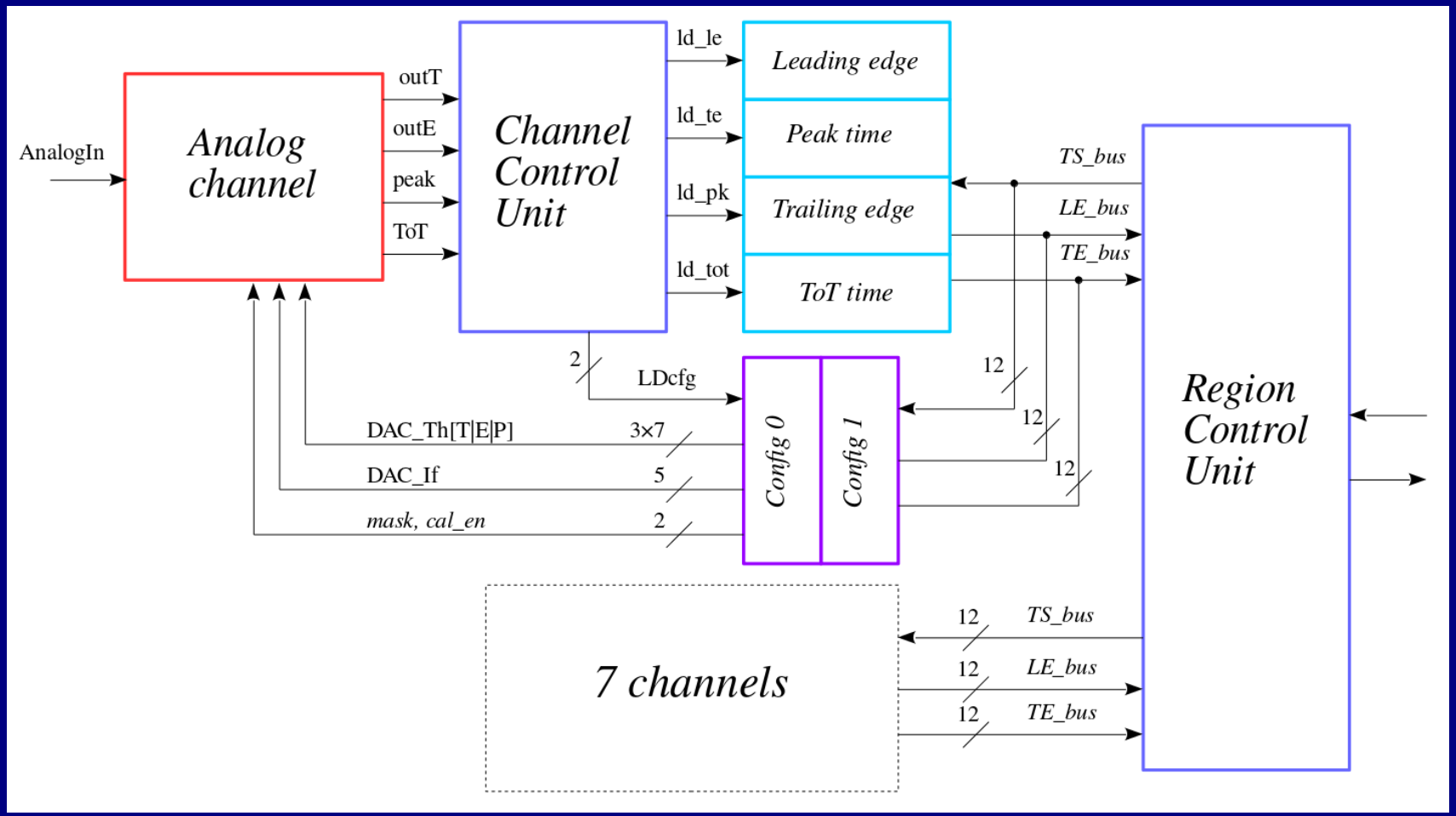
Analog front-end

- Charge Sensitive Amplifier
  - Fours gains : 2,6,8 and 12 mV/fC
  - Possibility to accept inputs from both polarities
- Shaper
  - 3^{rd} order, one real and two cc poles
  - Programmable peaking time : 25, 50, 150 and 250 ns
- Double threshold signal detection
  - Lower threshold for time measurement, higher threshold for validation
- Peak detector and holder
- Two ToT measurements
  - From leading and trailing edge times
  - From peak and ramp crossing times

Signal detection



Full channel architecture

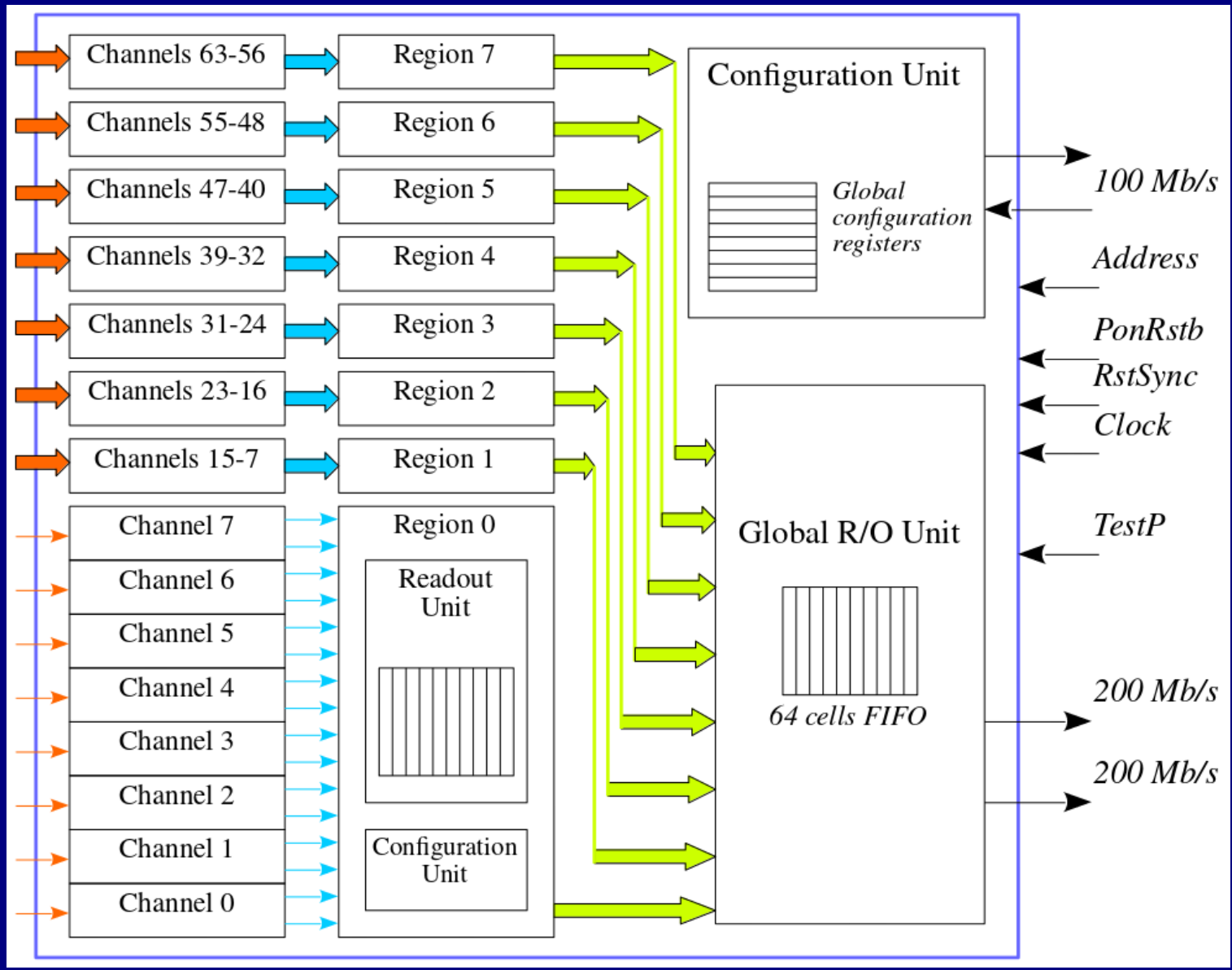


- Common time stamp
- 4 data register for time acquisition
- 2 configuration registers
- Thresholds and discharge current DACs

Time measurement

- Time resolution set by clock frequency
  - 200 MHz $\rightarrow$ 1.44 ns r.m.s.
- ToT-based charge measurement for time walk correction
- Option for second version
  - Channel or region-level 8-tap delay line
  - Delay controlled by a global DLL
  - Time resolution 180 ps r.m.s.
- Studies ongoing real signals
  - Problem of multiple ionization
  - Detector-FE co-design

ASIC architecture



Readout scheme

- Event driven (no trigger)
- Time of arrival order is different from time of readout
- Events are divided in frames
  - Frame duration : full cycle of the time-stamp counter
  - Event readout order does not correspond to event time of arrival
  - Events in a given time frame are not time-ordered
  - Events belonging to the same time-stamp counter cycle are transmitted in the same frame
- Continuous data transmission *(sync words when no data available)*

Output data format

- Data output in 32 bits words over 1 or 2 serial links @ 200 Mb/s
- Two 32-bit words per event (one in LeTe mode)
- Frame : rollover time for the time stamp counter, i.e. 20.48 μs at 200 MHz
- Data within a frame are packed within a frame header and a frame trailer
- Frame header contains chip id and frame number
- Frame trailers contains the number of valid samples and CRC

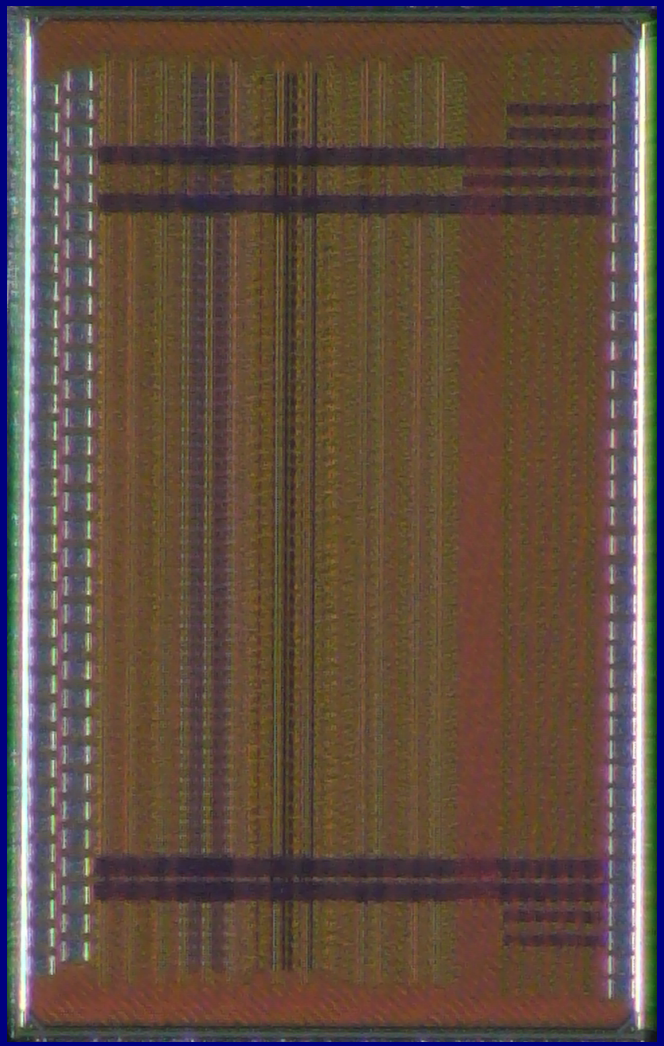
Packet type	Header *2 bit*	Data *30 bits*			
Data word 0	10	Region[2:0]	Channel[2:0]	Le[11:0]	Te[11:0]
Data word 1	11	Region[2:0]	Channel[2:0]	Pk[11:0]	ToT[11:0]
Header	01	01	*Reserved[12:0]*	ChipId[6:0]	FrameN[7:0]
Trailer	01	10	DataCnt[11:0]		CRC[15:0]
Sync	00	00	1100 1100 1100	1100 1100 1100	1111

ToRA configuration

- Data input and output in 16 bits words over 100 Mb/s serial links
- 7 bit address (from external pads)
- Broadcast address (write only)
- 18 Global Configuration Registers (GCR)
- 2×64 Channel Configuration Registers (CCR)

Function	**Data** 4 bits	**Op code** 12 bits
Chip Select	1101	$01a_B a_6 a_5 a_4 a_3 a_2 a_1 a_0 00$
Chip Deselect	0000	00xx xxxx xxxx
Register select (channel)	0100	$0000 r_2 r_1 r_0 0 c_2 c_1 c_0 a_0$
Register select (region)	0100	$0000 r_2 r_1 r_0 1 a_3 a_2 a_1 a_0$
Register select (global)	0100	$00010 a_6 a_5 a_4 a_3 a_2 a_1 a_0$
Register write	0101	$d_{11} d_{10} d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$
Register read	0110	0000 0000 0000
No operation	1111	0000 0000 0000
GCR read word	1000	$d_{11} d_{10} d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$
Channel register read word	1010	$d_{11} d_{10} d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$

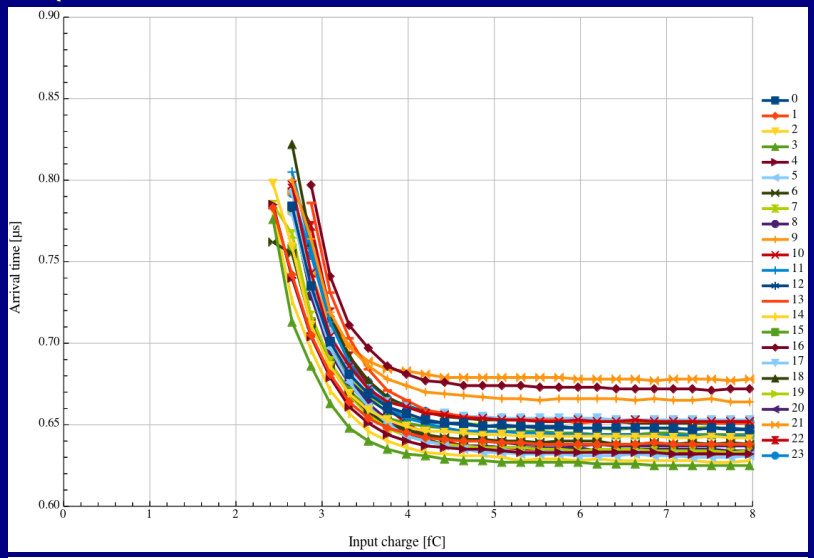
ToRA v1 prototype

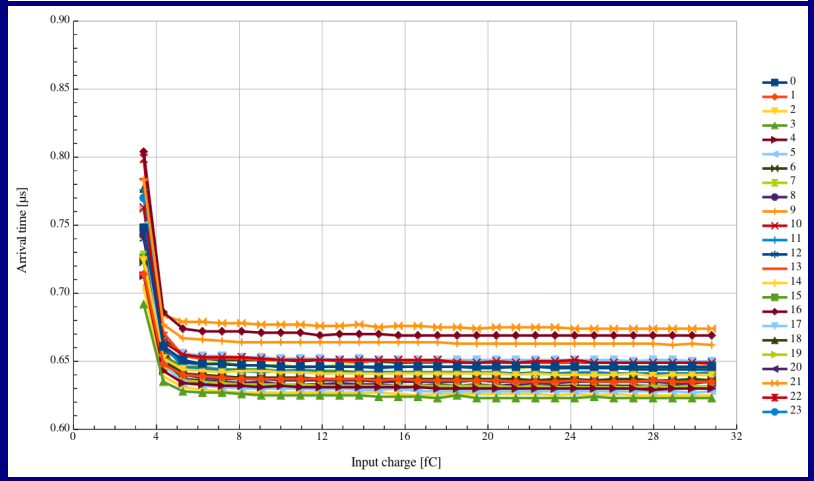


- 64 channels
- 4 gains, 4 shaping times
- Clock frequency : 200 MHz
- ToA and TtoPeak measurement
- Simple and linear ToT measurement
- Single external voltage reference
- Fully differential configuration and data transmission
- Die size : 2.6×4.3 mm^2
- CMOS 65 nm technology
- Three power supplies (analog, digital, I/O) @ 1.2 V
- Power consumption $\sim$600 mW

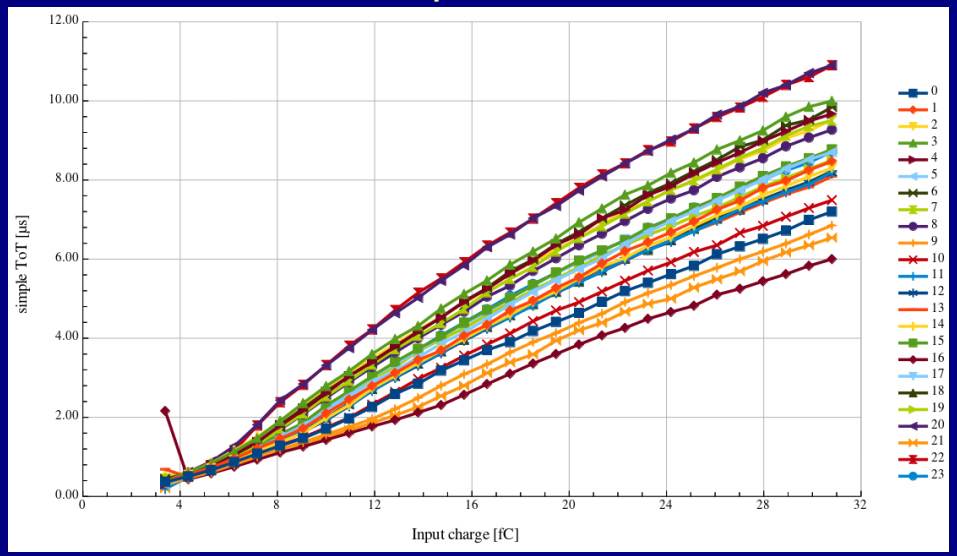
(Very) preliminar test results

ToA (normal and extended test pulse range)





simple ToT



- Raw data : no gain and threshold calibration applied yet
- No data on peak detection and linear ToT available yet
- Maximum gain and peaking time

Conclusions

- ToRA is a new ASIC for the readout of MicroMegas detectors
- Custom developed analog FE
- Four gains : 2,6,8 and 12 mV/fC
- Four peaking times : 25,50,150 and 250 ns
- Provides ToA, peak position, ToT
- Digital BE from a silicon-proven design (ToASt)
- Submitted on May 2025, received on September 2025
- Status : under test
  - Digital interface ok
  - First results on analog behaviour
  - *Still a lot of work for full characterization*