6th DRD1 Collaboration meeting

FATIC readout electronics for the LHCb upgrade 2 muon system

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on behalf of the LHCb Collaboration

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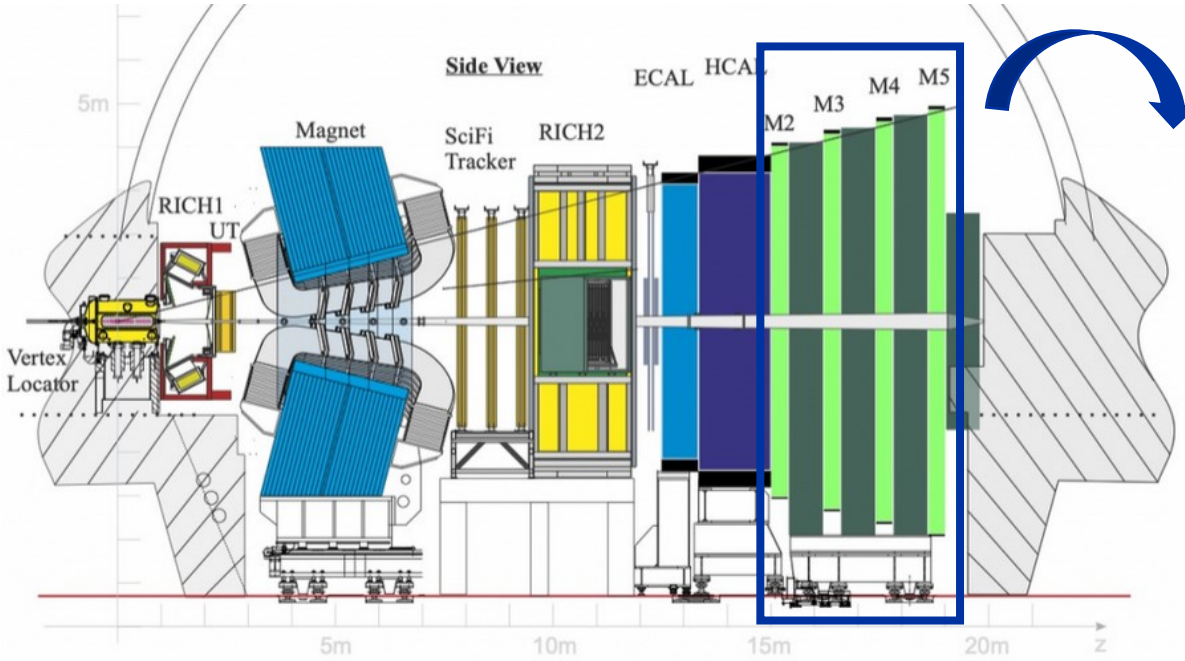
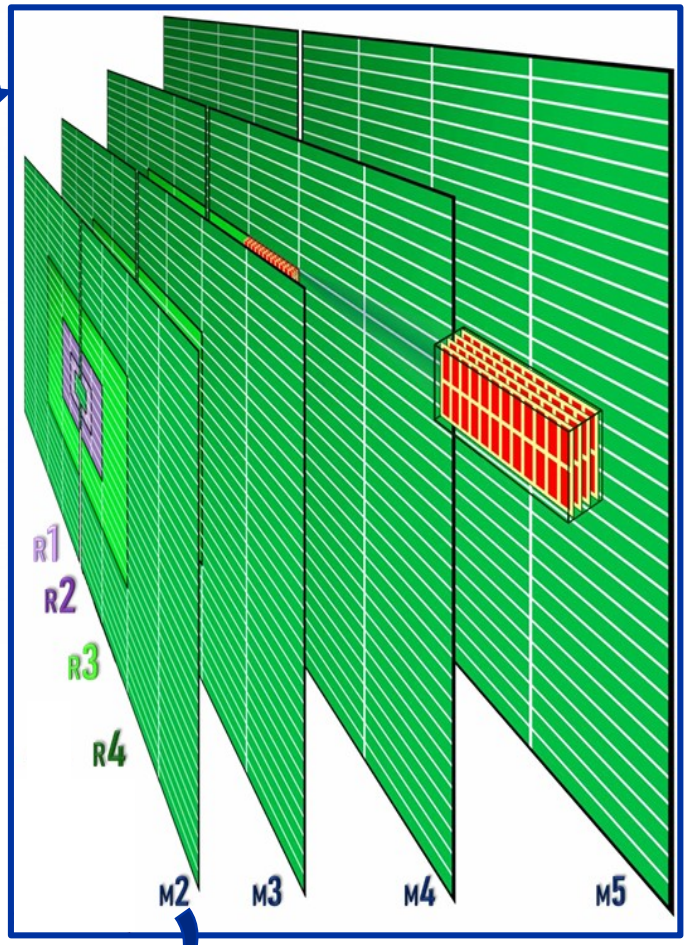
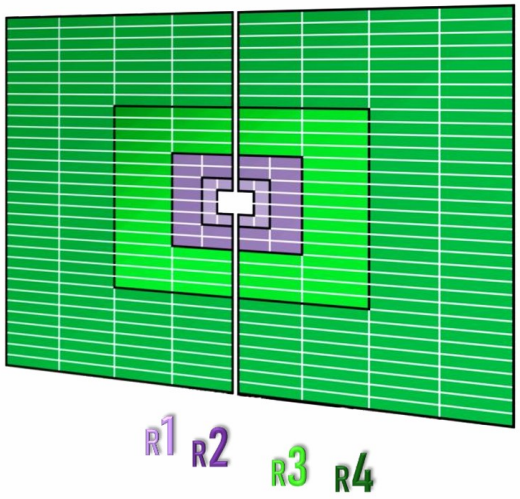
The LHCb muon system







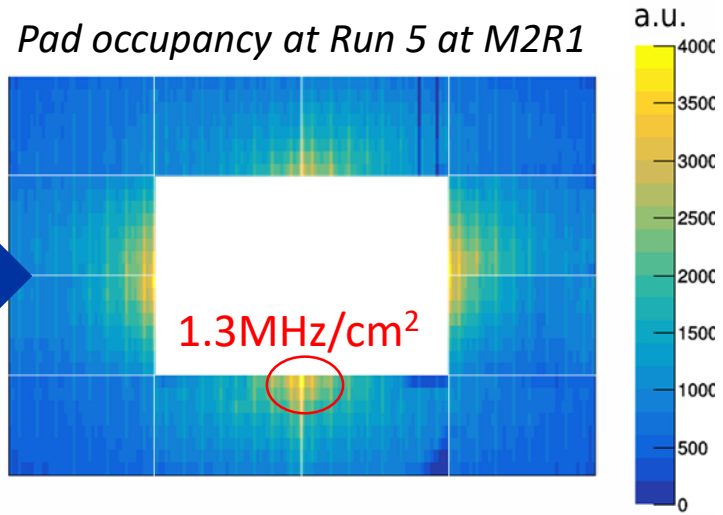
- 4 stations (M2-M5) interleaved with iron absorbers
- Each station is divided in 4 regions (R1-R4) equipped with 4-gaps Multi Wire Proportional Chambers

The muon system at HL-LHC

Currently: LHC Run 3 with $L=2\cdot10^{33}$ $cm^{-2}s^{-1}$
Maximum rate < 100kHz/cm²

From 2036: LHC Run 5 with $L=1\cdot10^{34}$ $cm^{-2}s^{-1}$

Pad occupancy at Run 5 at M2R1



LHCb muon system upgrade 2 for HL-LHC:

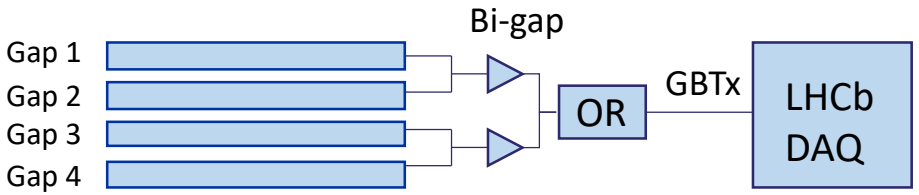
- Background rate reduction: addition of a shielding in place of HCAL calorimeter and **new readout scheme**
- Sustain rates up to **~1MHz/cm²** in R1-R2:
  - increase of detector granularity (max **700 kHz/ch** expected)
  - **new detectors with high rate capability and new front-end electronics**
- Reuse of most of the present MWPCs in R3-R4. Replace of some MWPCs foreseen: new MWPCs with higher granularity under production.

Maximum per region of the chamber average rates expected at Run5

kHz/cm2	R1	R2	R3	R4
M2	660.9	153.5	25.9	9.3
M3	219.8	38.2	4.7	1.6
M4	184.4	22.6	3.2	0.8
M5	155.6	13.2	2.9	2.2

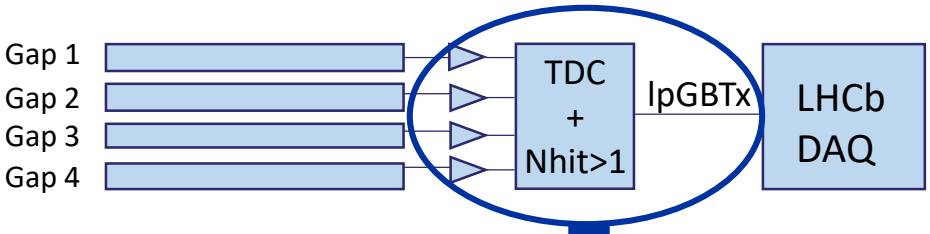
New readout scheme

Current readout scheme



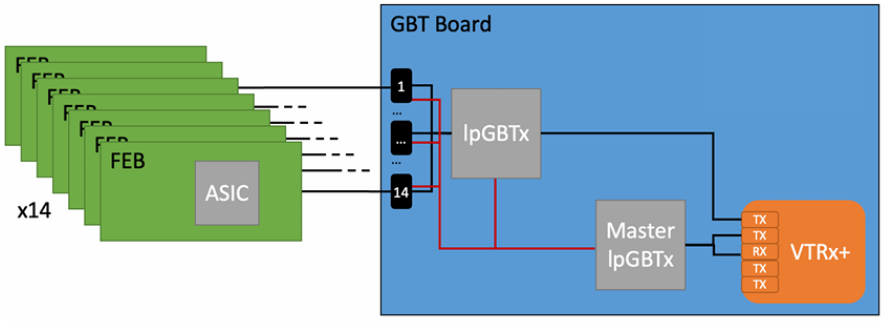
High rates at Run 5, mainly dominated by single-gap background signals. Reduction of uncorrelated bg hits required for U2

New readout scheme for U2



Expected reduction of the background by a factor $\mathbf{2 \div 4}$ (depending on region/station) at the cost of small efficiency loss for muon detection (-1 % per station)

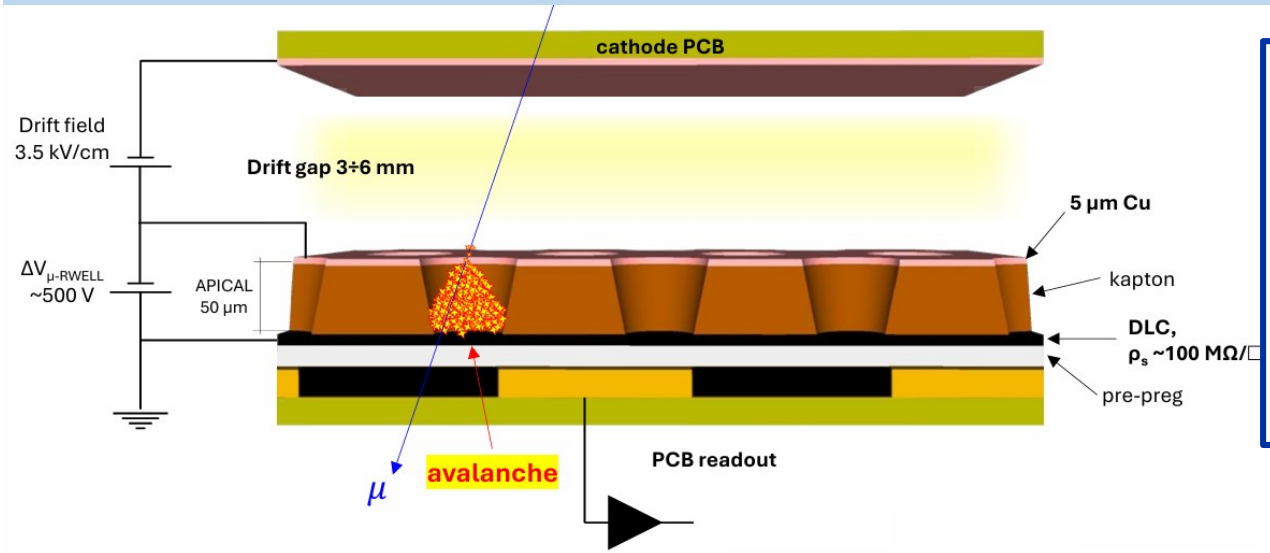
P. Albiccoco, FEE@U2 workshop



- FE chips connected to 64 channels: about 13k ASICs in total.
- Specific links dedicated to Data and to TFC/ECS (2 lpGBTx per GBT board)
- Up to 14 FE chips per data lpGBTx via 1 eLink @ 640MHz : Total FE Bandwidth 8.5Tbps

New muon detectors for high rates

A MPGD detector: Micro-resistive WELL (μRWELL)

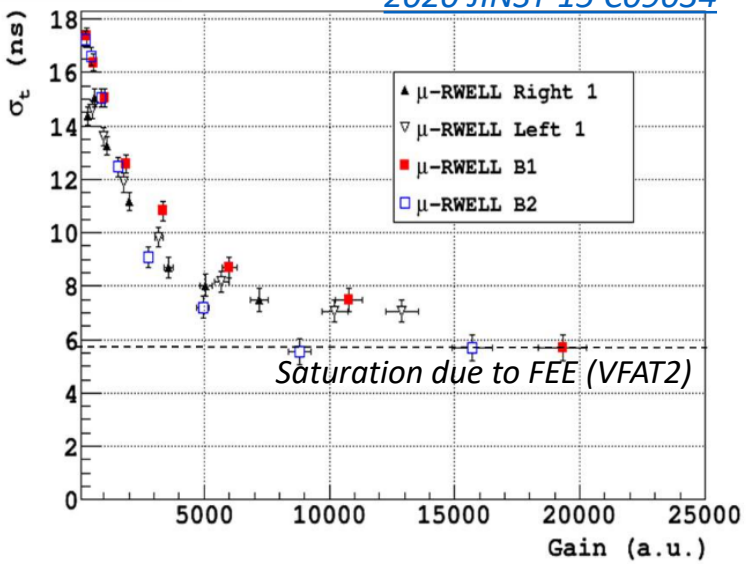


- Ionisation from drift region amplified in well foil (Cu+Kapton), generating an avalanche.
- Discharges suppressed by the DLC resistive layer.
- Pad readout

Typical charge signal of O(10fC). FEE:

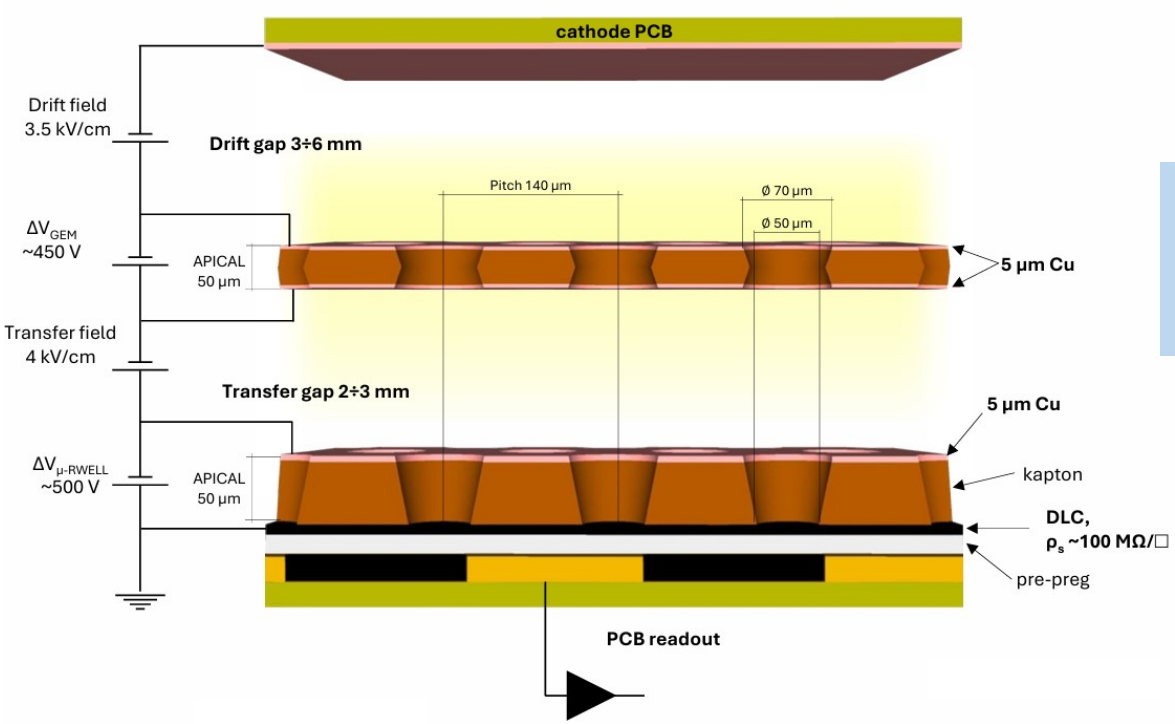
- First tests performed with VFAT2, used for example for GEM readout: need of «faster electronics»
- Efforts concentrated on FATIC chip, designed by INFN Bari for the processing of signals with sub-ns duration and charge content at the level of 1fC readout from FTMs

2020 JINST 15 C09034



New muon detectors for high rates

An evolution of the µRWELL: GRWELL



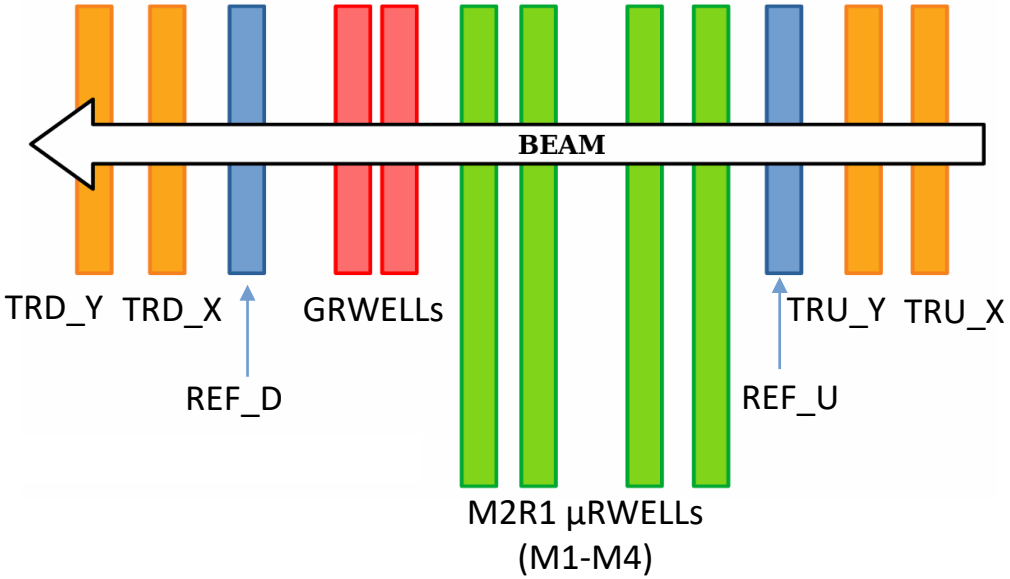
GEM foil added to the µRWELL drift region

Two amplification stages: GEM Pre-amplification + μRWELL amplification
Larger gas gain (>> 10^4) in very stable conditions.

Detectors based on µRWELLs and GRWELLs readout by FATIC FE boards have been tested.

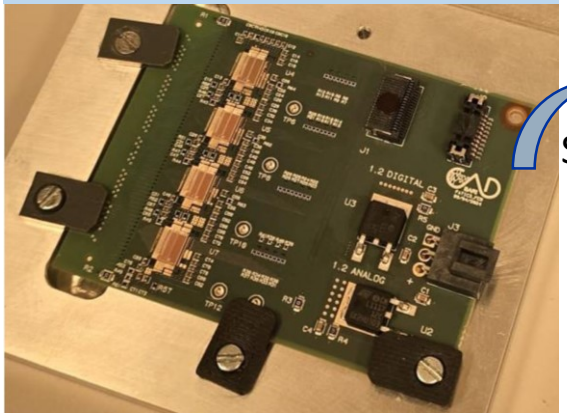
Test beam campaign

A test campaign has been carried out in 2024 at PS T10 beam line with 5GeV muons



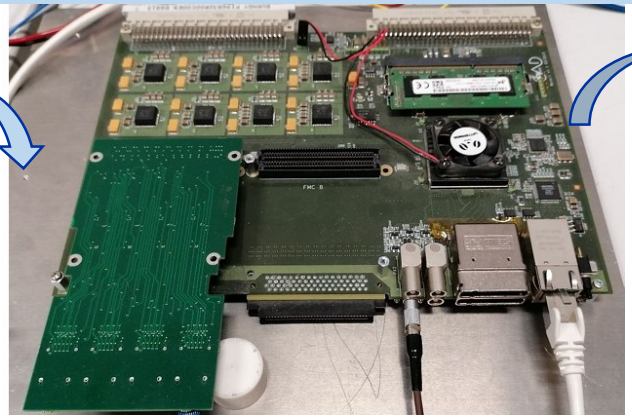
- 4 tracking µRWELLs with strip R/O
- 2 reference µRWELL chambers
- 4 prototypes for M2R1 µRWELLs (30x25)cm^2 - 9x9 mm^2 pad R/O
- 2 GRWELLs under test (10x10)cm^2 – 9x9 mm^2 pad R/O
- Gas mix.: 45%Ar/ 15% CO_2/40% CF_4
- Trigger provided by the coincidence of 2 perpendicular scintillators with the PS T10 scintillators

16 FE boards each hosting 4 FATICs



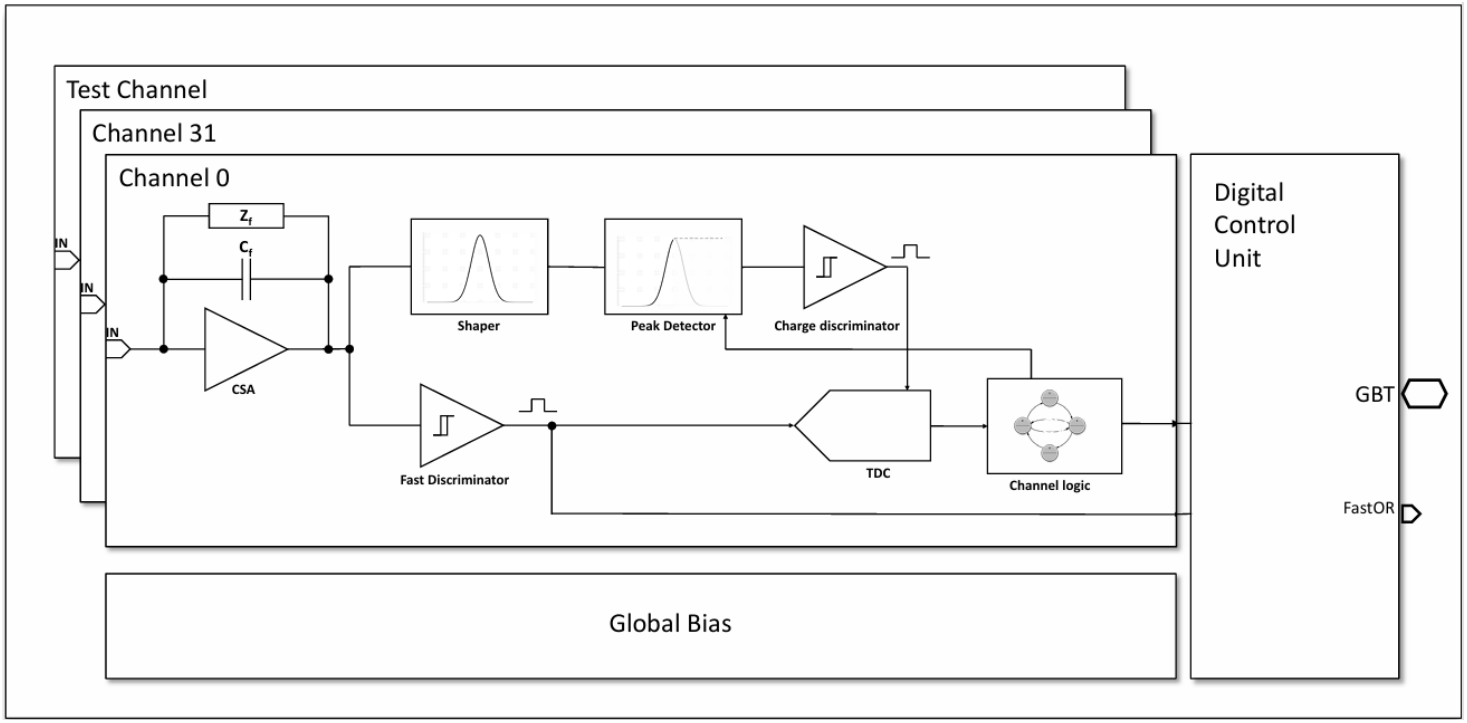
SLVS

3 MOSAIC boards acquiring data + 1 MOSAIC acting as master for the distribution of the 40MHz clk, sync and trigger



ethernet

FATIC ASIC



- FAst Timing Integrated Circuit (FATIC) designed in TSMC 130 nm technology
- CSA with programmable polarity, gain (10 mV/fC, 50 mV/fC) and recovery time
- Shaper with programmable peaking time: 25 ns, 50 ns, 75 ns, 100 ns
- Charge measurement with dynamic range > 50 fC and programmable charge resolution
- Time measurement (ToA) using 100 ps TDC
- 640 Mbps serial link, LpGBT compatible
- Power consumption ~200 mW

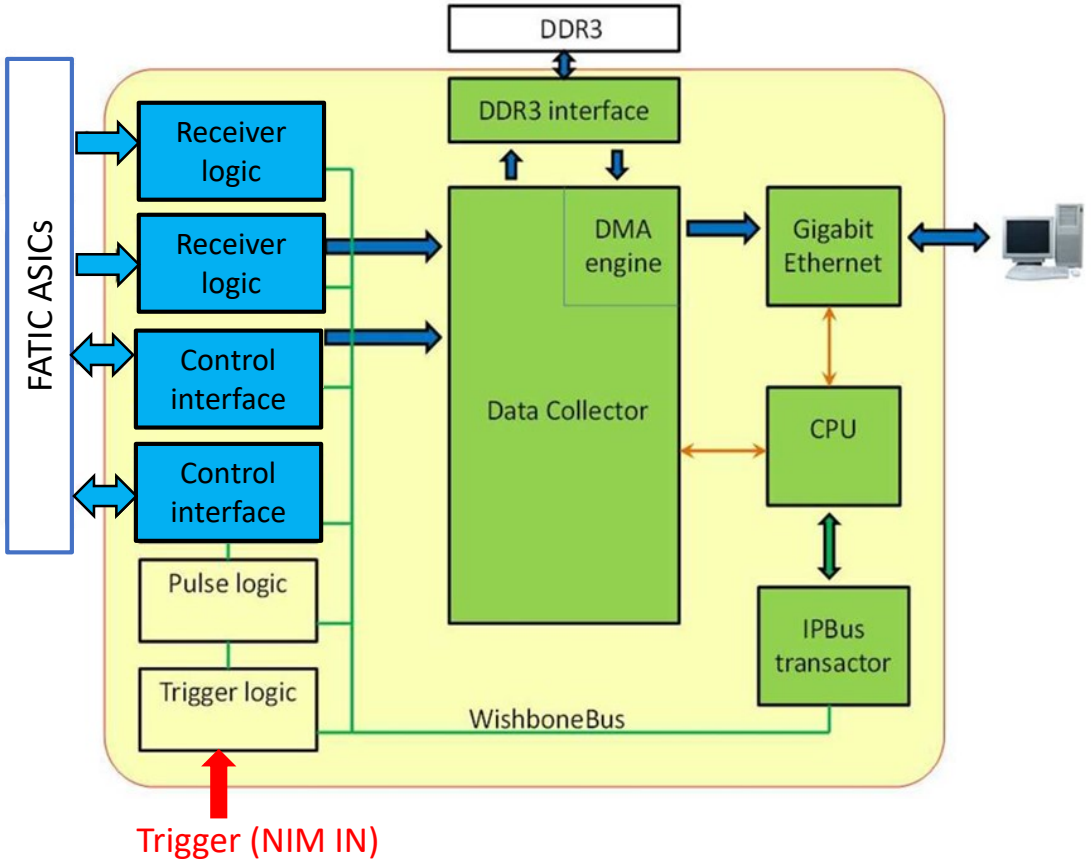
MOSAIC board

Artix-7 FPGA with a Modular System for Acquisition, Interface and Control (MOSAIC) firmware developed by INFN Bari

«Flexible» structure:

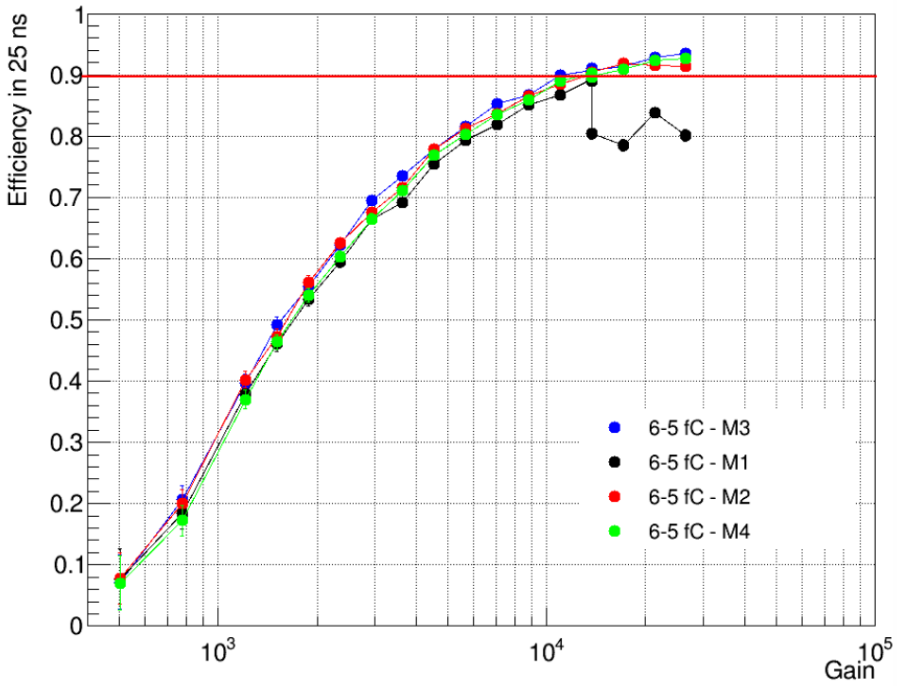
- **Infrastructure:** Wishbonebus for configuration and monitoring + interface for DDR3 memory
- **Hardware-dependent modules**

Software dedicated to data acquisition performing also the configuration and monitoring of FATIC and MOSAIC boards developed

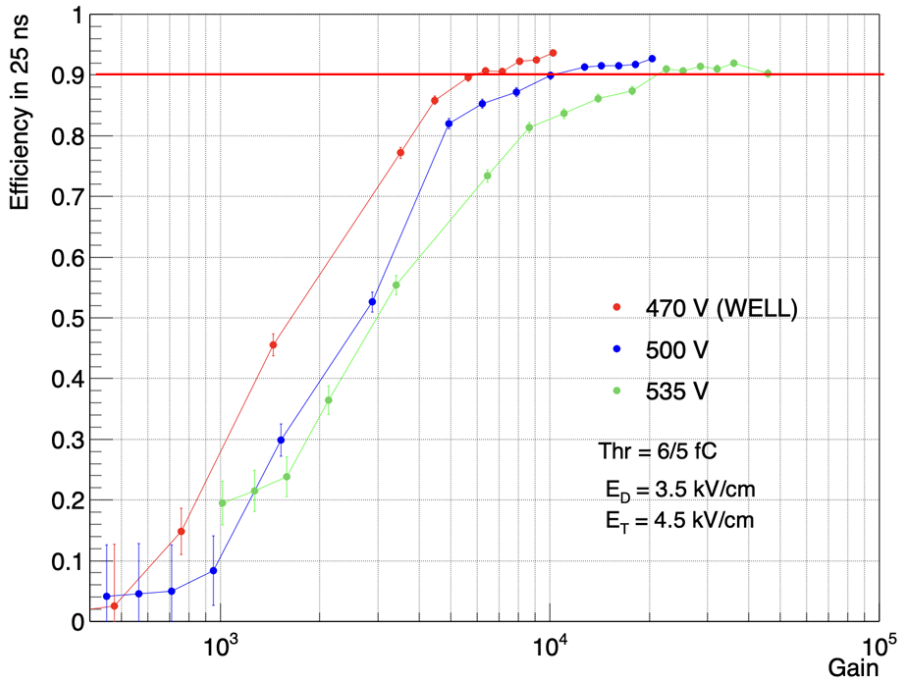


Test beam results

Efficiency for M2R1 µRWELLs readout by FATIC



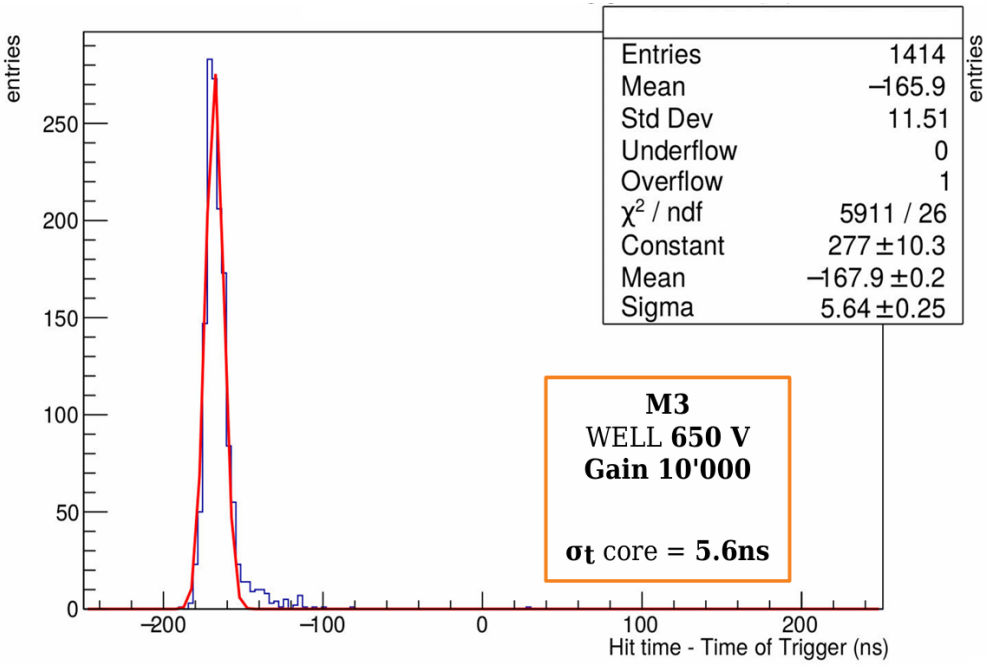
Efficiency for a GRWELL readout by FATIC



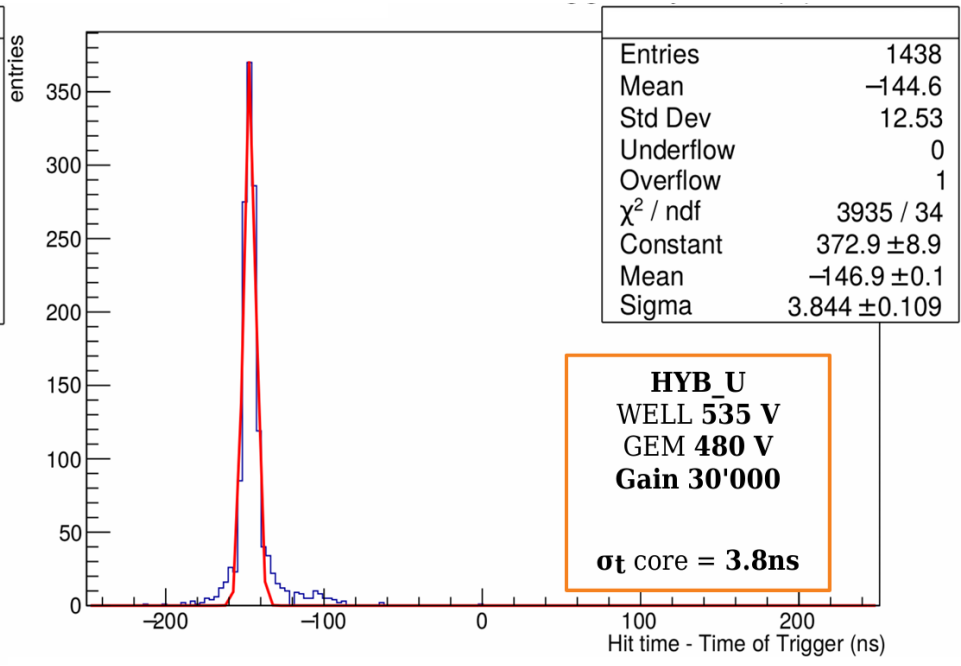
A single-gap efficiency of 90% within 25 ns is reached at gas gain of 10^4 , which is close to the typical max gain of the µRWELL, but is well within safe detector operational limits for GRWELL.

Test beam results

Time resolution for M3 µRWELL readout by FATIC

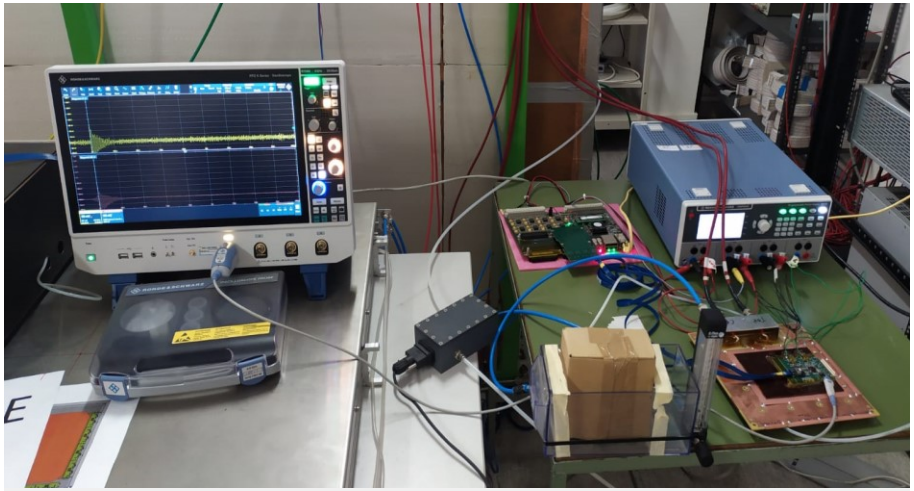


Time resolution for a GRWELL readout by FATIC

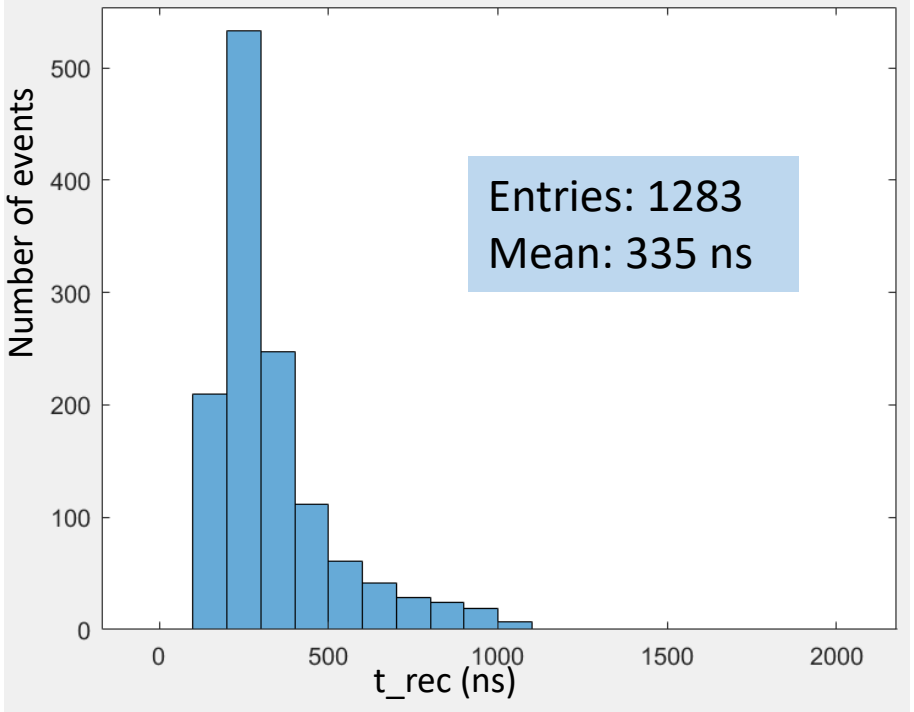


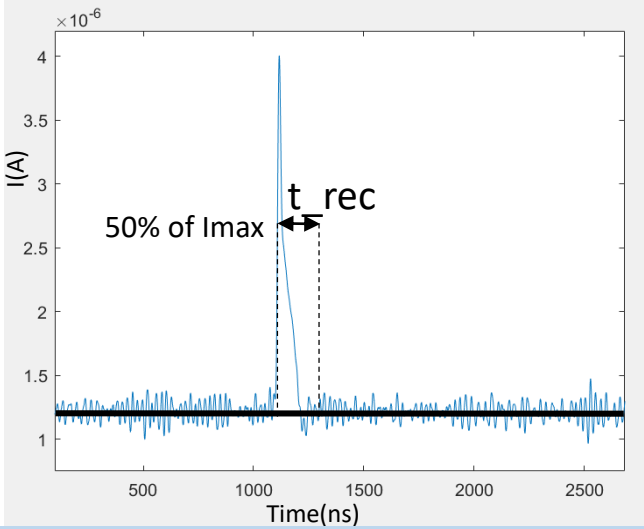
The GRWELL readout by FATIC ASIC is currently regarded as the baseline for the LHCb muon system upgrade 2 in the most exposed regions (R1-R2).

Measurement of GRWELL signal



- Measurements with cosmic rays
- GRWELL gain ~ 10^4
- Oscilloscope acquiring 1Gsa/s from the test point of the FATIC CSA
- In order to prevent possible pile-up effects during operation at LHCb, focus on the eventual presence of signal tails : large signals studied (amplitude > 500mV).

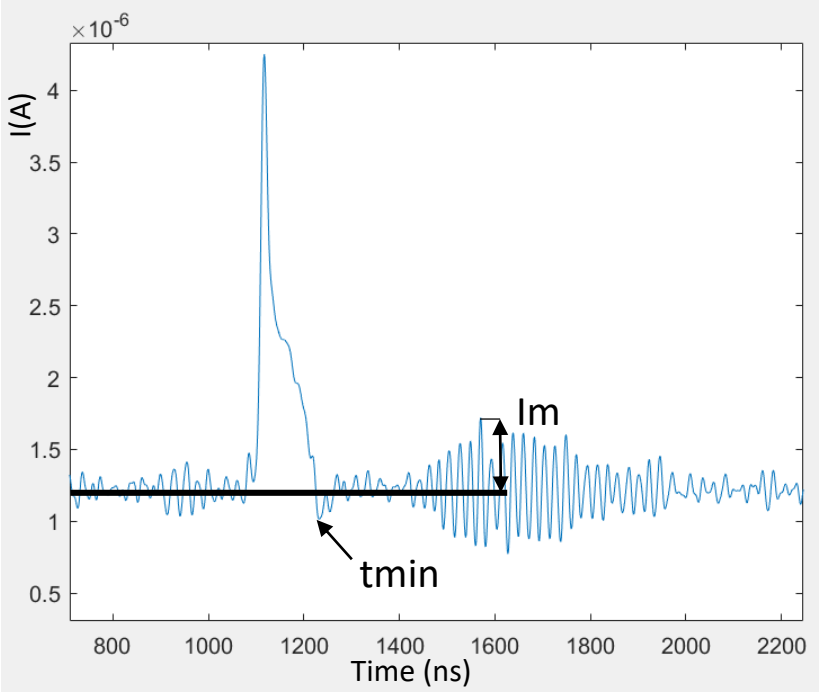


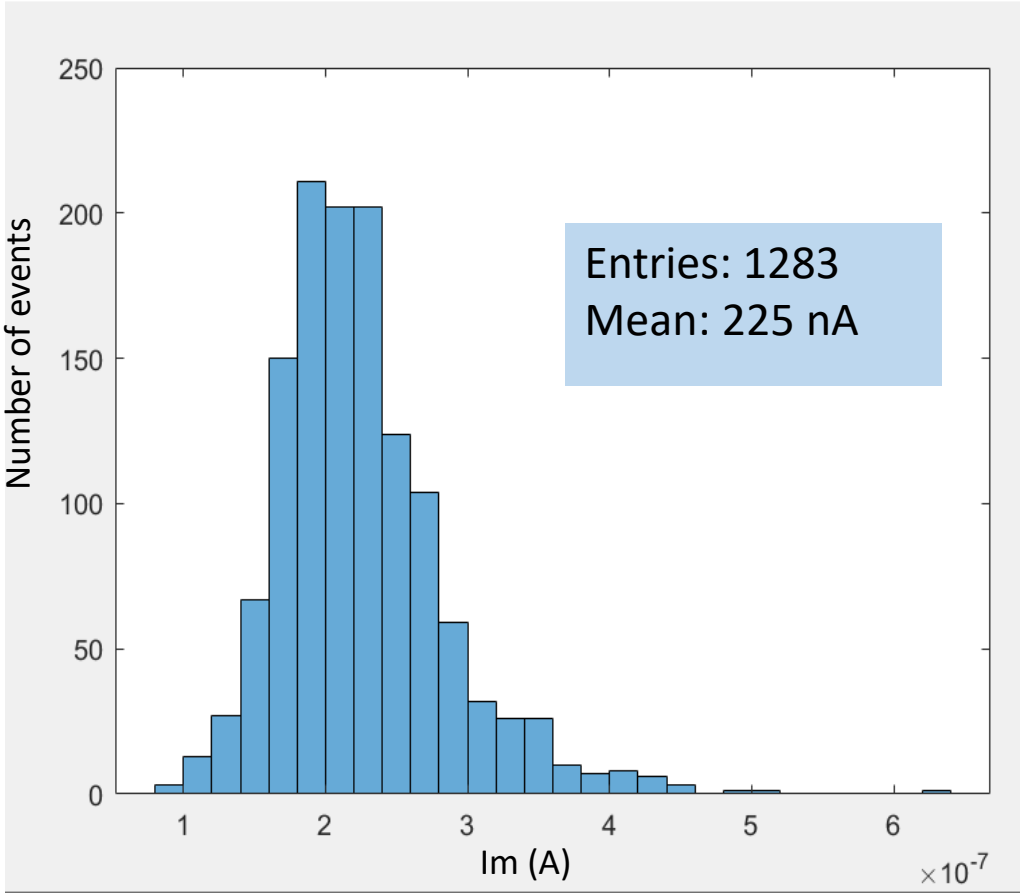


- t_rec: recovery time at which current is comparable with the baseline (within 2nA)
- It is approximately within 1 µs

Measurement of GRWELL signal

Im: maximum current value for time in [tmin,tmin+1μs] w.r.t. the baseline value

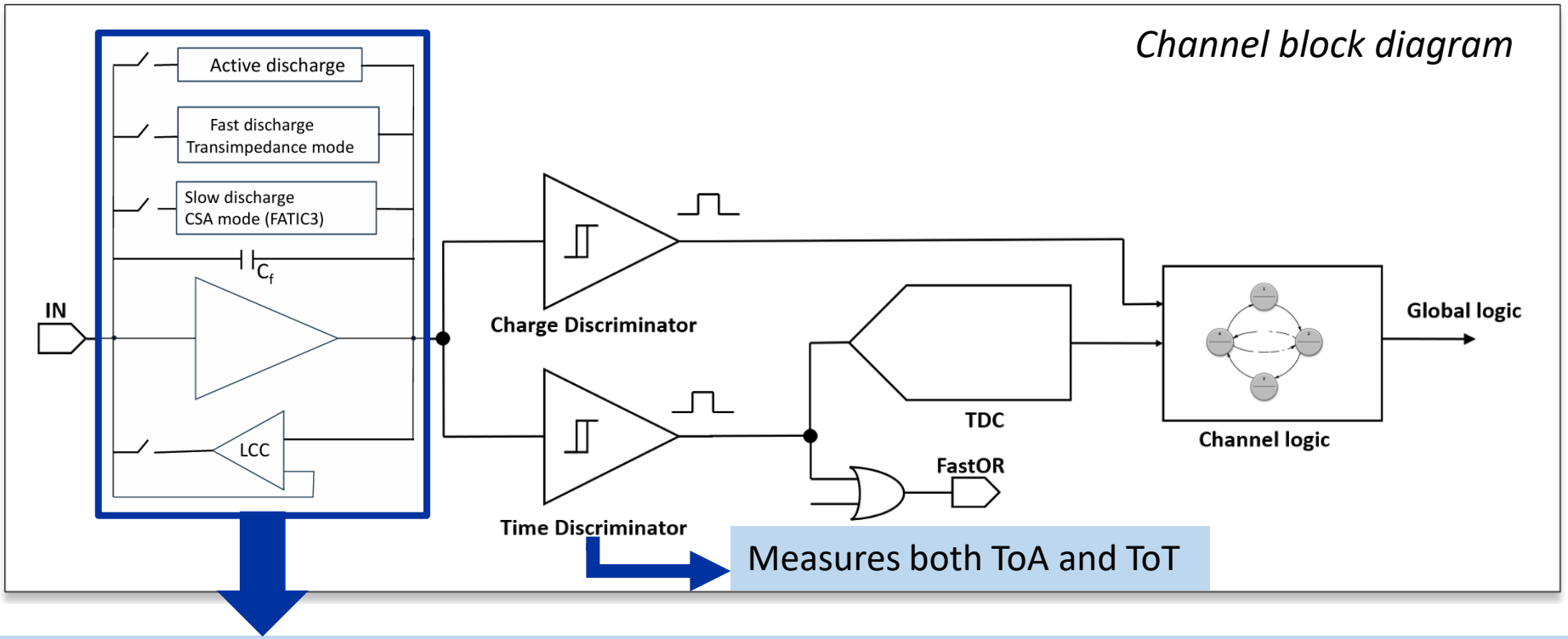




No clear sign of signal tail is spotted: signals reach values comparable with the baseline within ~1μs and in this time interval the maximum current measured (Im) is at the level of few hundreds of nA (~5% of current amplitude), biased by the noise level which could reach ~500nA.

A new FATIC version

The current FATIC chip has a dead time of ~1µs, mainly driven by the CSA, which should be reduced up to 100ns in order to guarantee efficient operations at the expected rates (~700kHz/ch): a new FATIC version is under development.

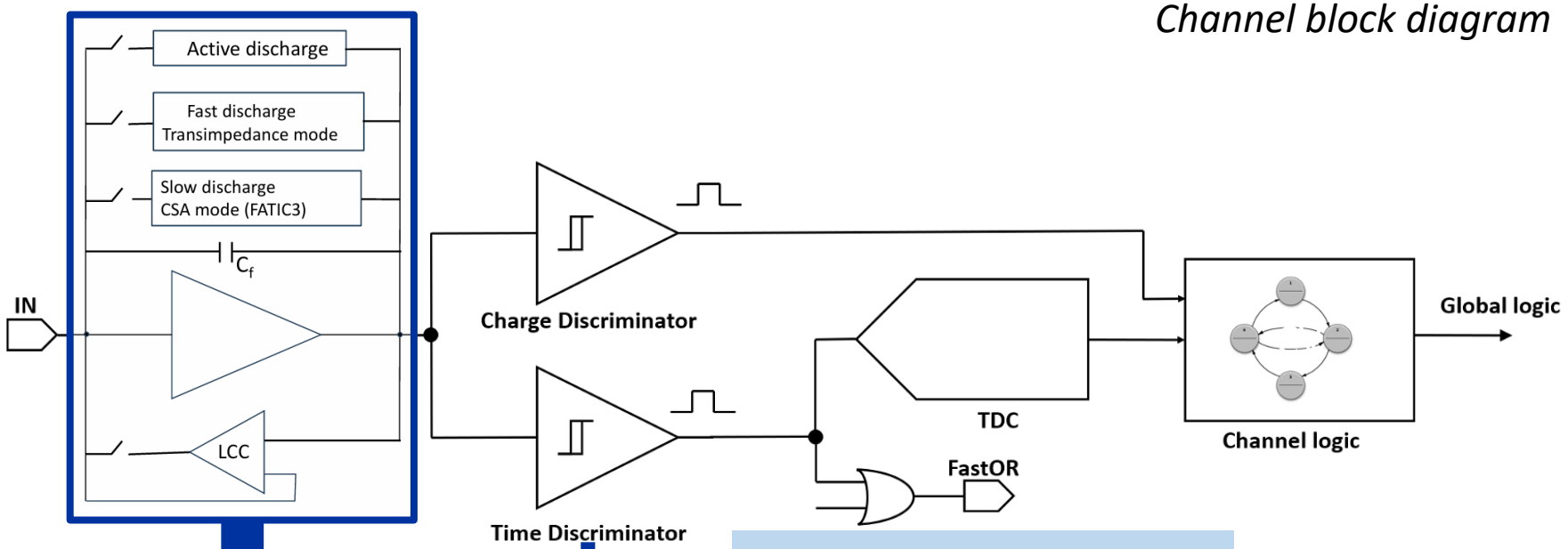


New preamplifier diagram:

1. **CSA mode** (the same of the previous FATIC version): programmable MOS discharge resistor. Fixed gain (7mV/fC), adjustable recovery time.

A new FATIC version

Channel block diagram

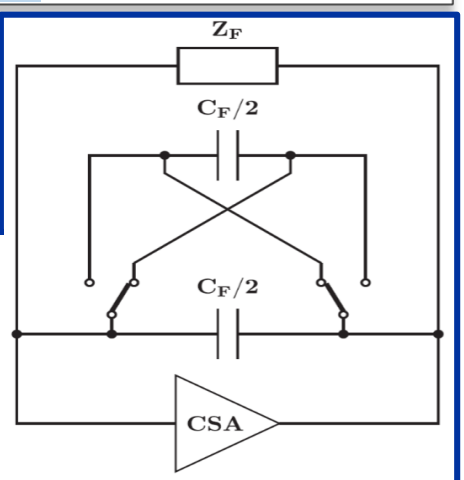


Measures both ToA and ToT

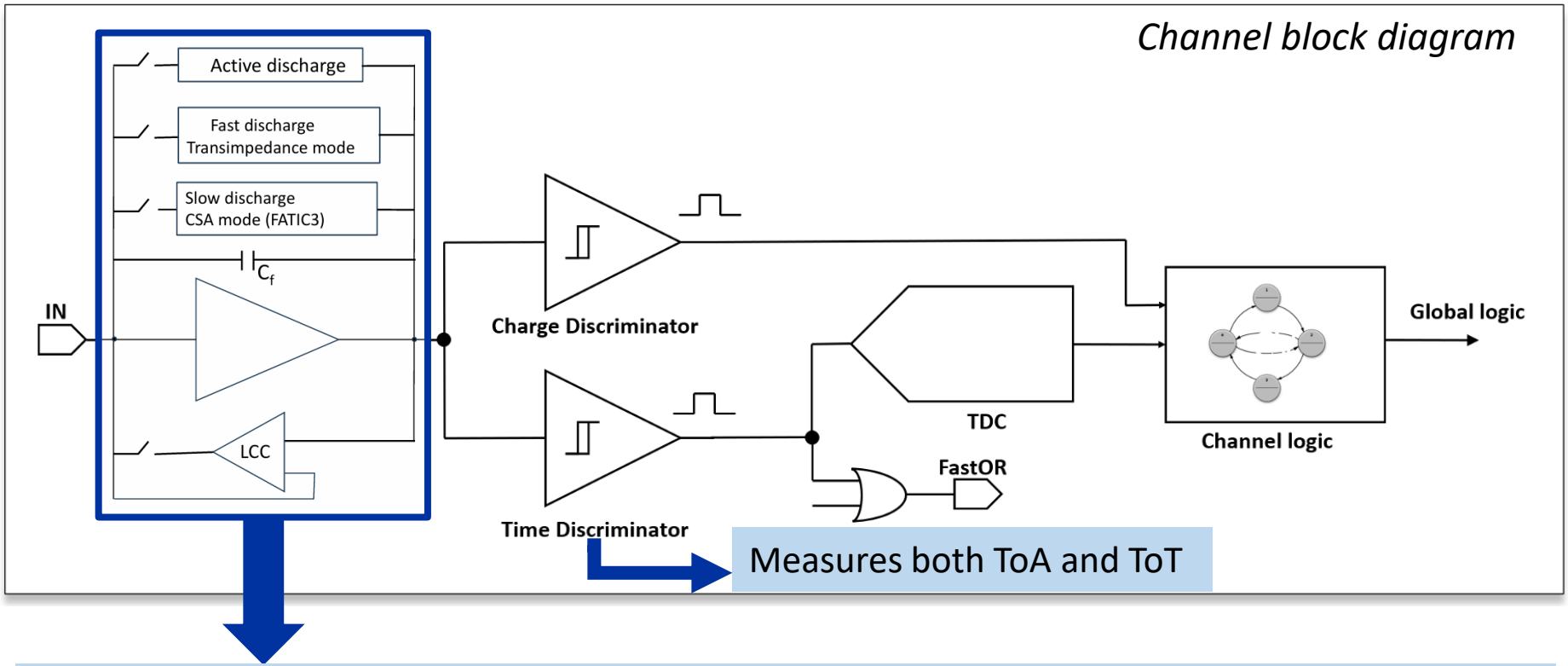
New preamplifier diagram:
2. **Fast reset** : speed-up the discharge process: **fast recovery<100 ns**

Fast discharge mode: Fixed R=200 kΩ in parallel to programmable MOS resistor to decrease τ in case of large signals

Active mode: digitally controlled, already implemented by R. Kleczek et al. in the in the SPC Pixel IC.



A new FATIC version

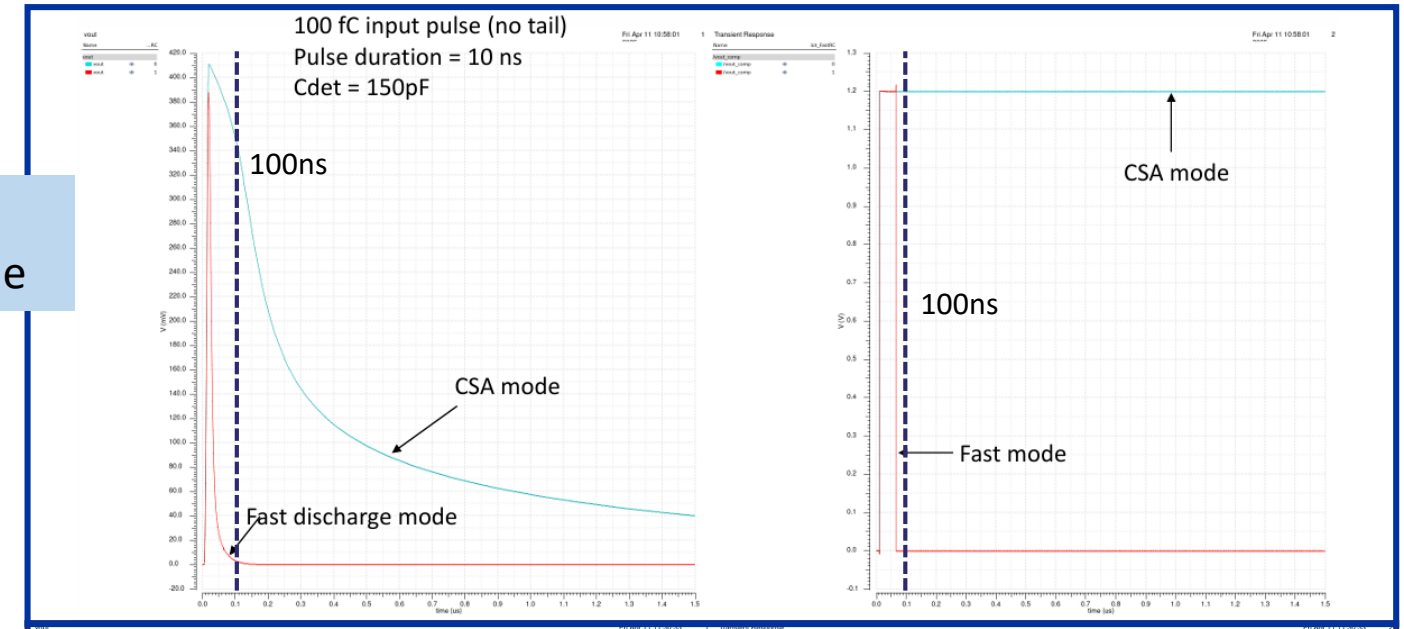


New preamplifier diagram:

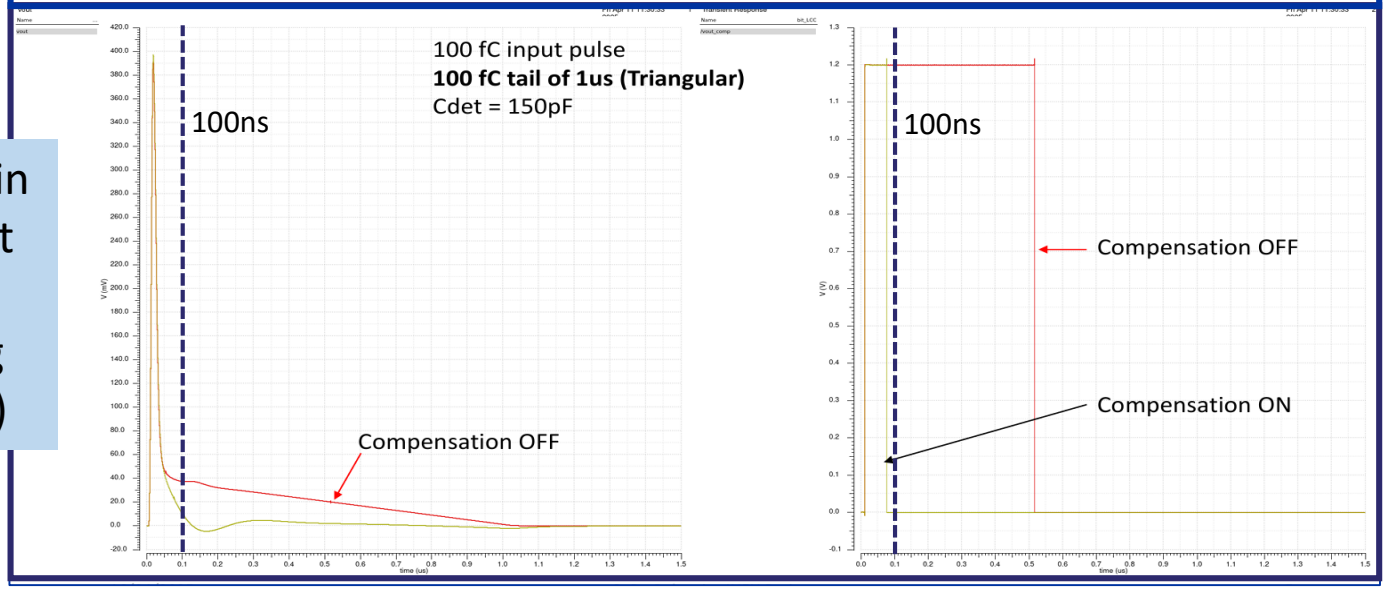
3. **Leakage-current compensation circuit (LCC)** with two programmable parameters (filter capacitance and LCC bias current) can be activated to compensate a constant detector leakage current and/or an ion tail.

Circuital simulation of the new FATIC

CSA vs Fast mode

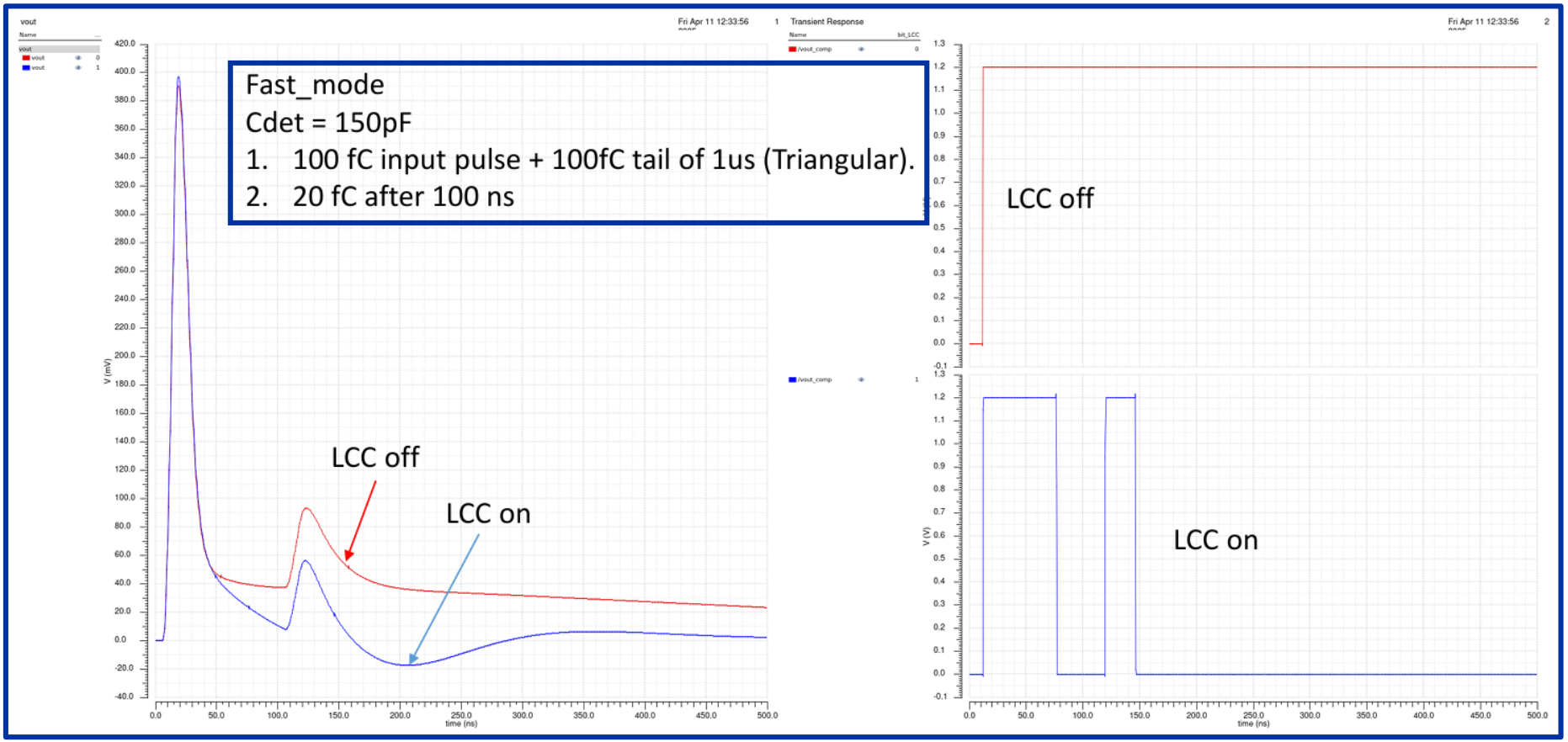


LCC effect in the «worst case» (including signal tail)



Circuital simulation of the new FATIC

Double pulse resolution



Conclusion

- The upgrade 2 of the LHCb muon system proposed for LHC Run 5 and beyond includes the installation of new GRWELL detectors in the most exposed regions (up to ~1MHz/cm^2 expected) readout by FAst Tuning Integrated Circuit (FATIC) ASICs.

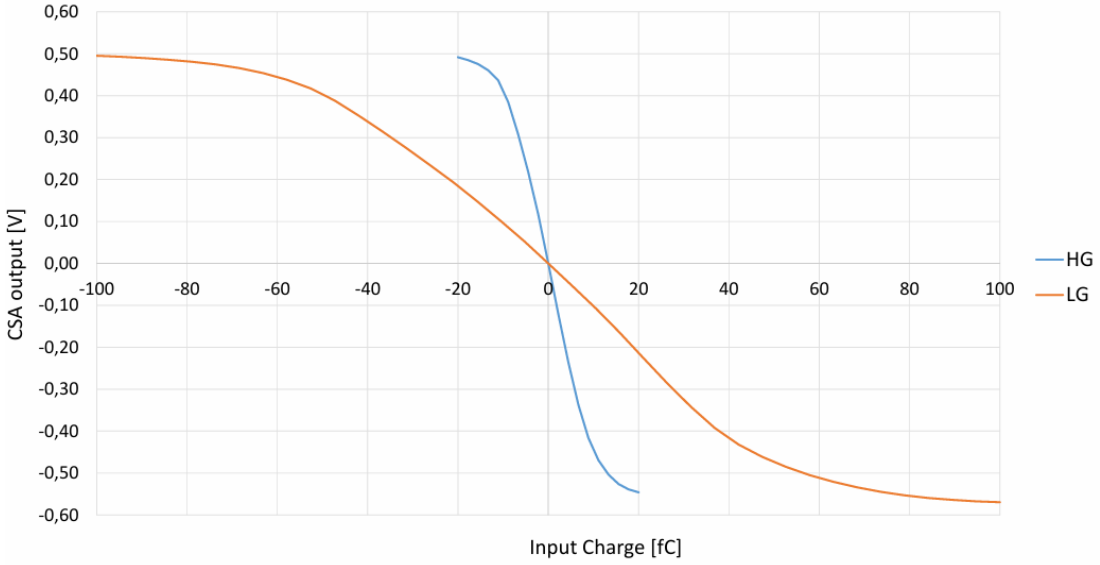
- Prototypes for the new detectors readout by FATIC chips have been tested at the PS T10 beam line showing promising results, namely a single-gap efficiency > 90% within 25 ns and a time resolution of 3.8 ns.

- In order to guarantee efficient operations at the expected signal rates (up to 700kHz/ch), an improved FATIC version with dead time reduced from 1µs to 100ns is being submitted in these weeks.

- A careful study has been performed to prevent pile-up effects.
  - dedicated measuremets of GRWELL signals acquired by FATIC: no clear sign of ion tail spotted.
  - A LCC circuit allowing to compensate a constant detector leakage current and/or an ion tail is anyway included in the new FATIC version.

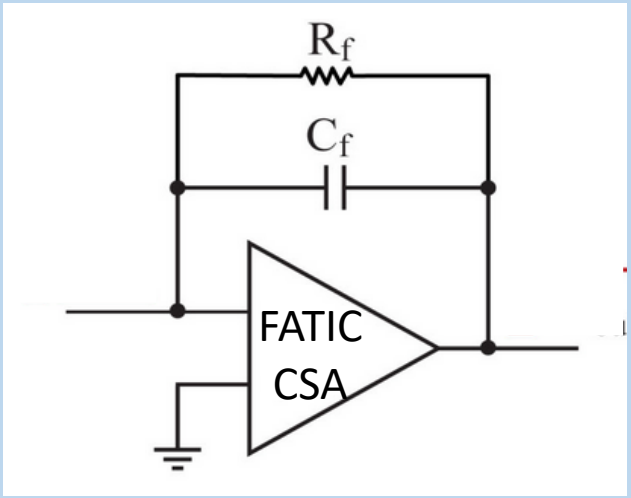
Thank you for your attention

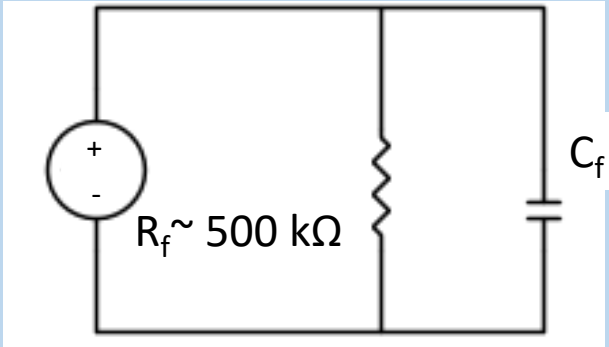
FATIC CSA



CSA output dynamic

Schematization performed for the analysis of the GRWELL signals





$$I = \frac{V}{Rf} + Cf\frac{dV}{dt}$$